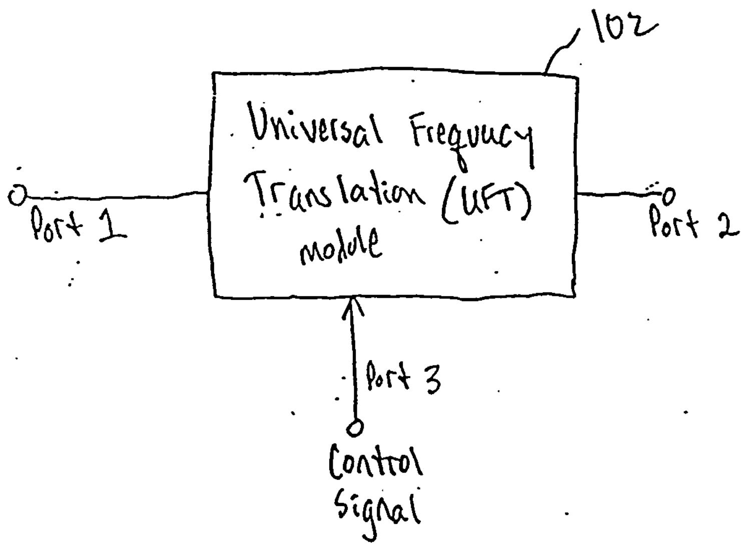
102
Universal Frequncy Translation (UFT) module
Port 1
Port 2
Port 3
Control Signal

FIG. 1A

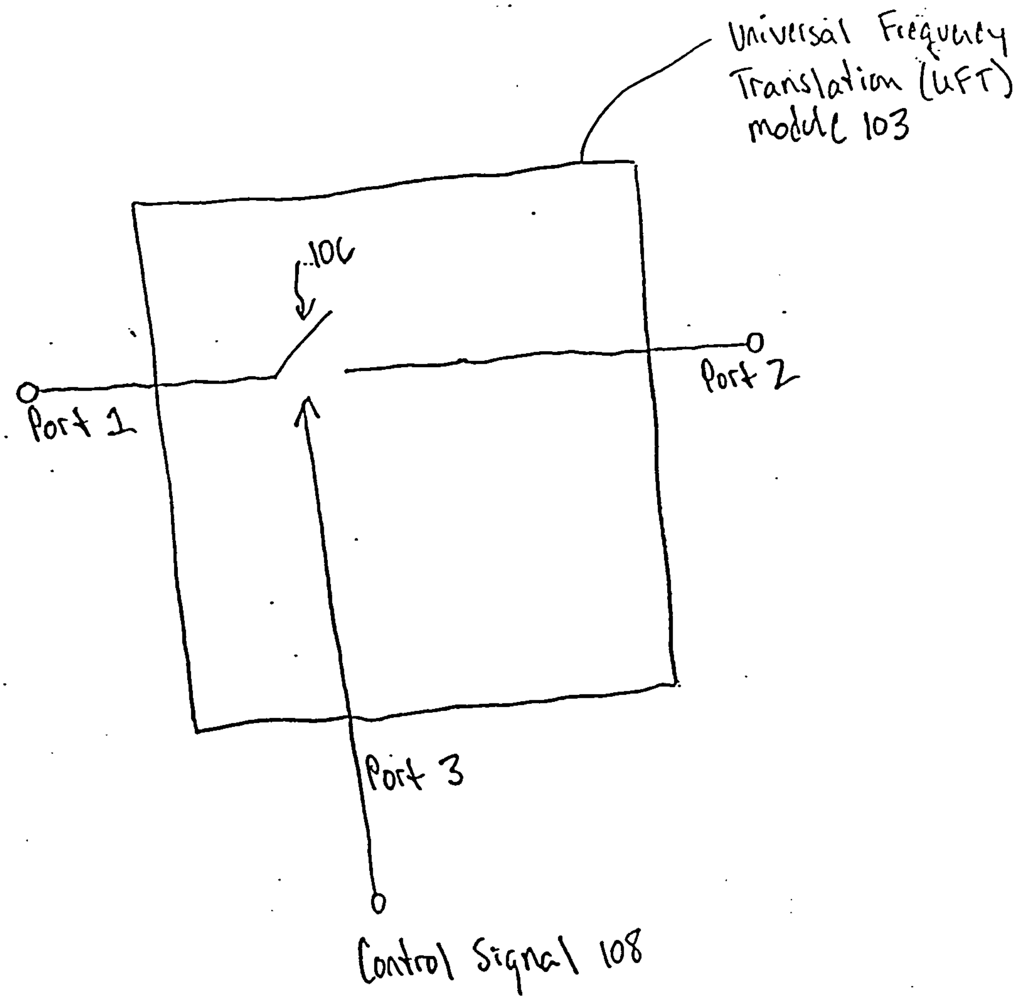
Universal Frequency Translation (UFT) module 103
106
Port 1
Port 2
Port 3
Control Signal 108

FIG. 1B

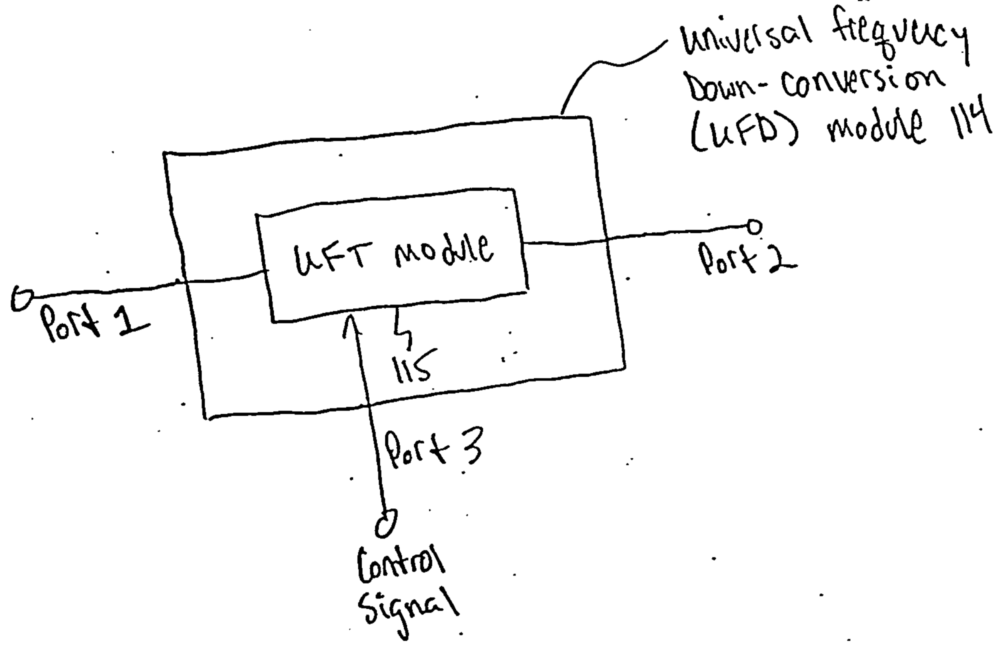
Universal frequency
Down-conversion
(UFD) module 114
UFT module
Port 1
Port 2
115
Port 3
Control
Signal

FIG. 1C

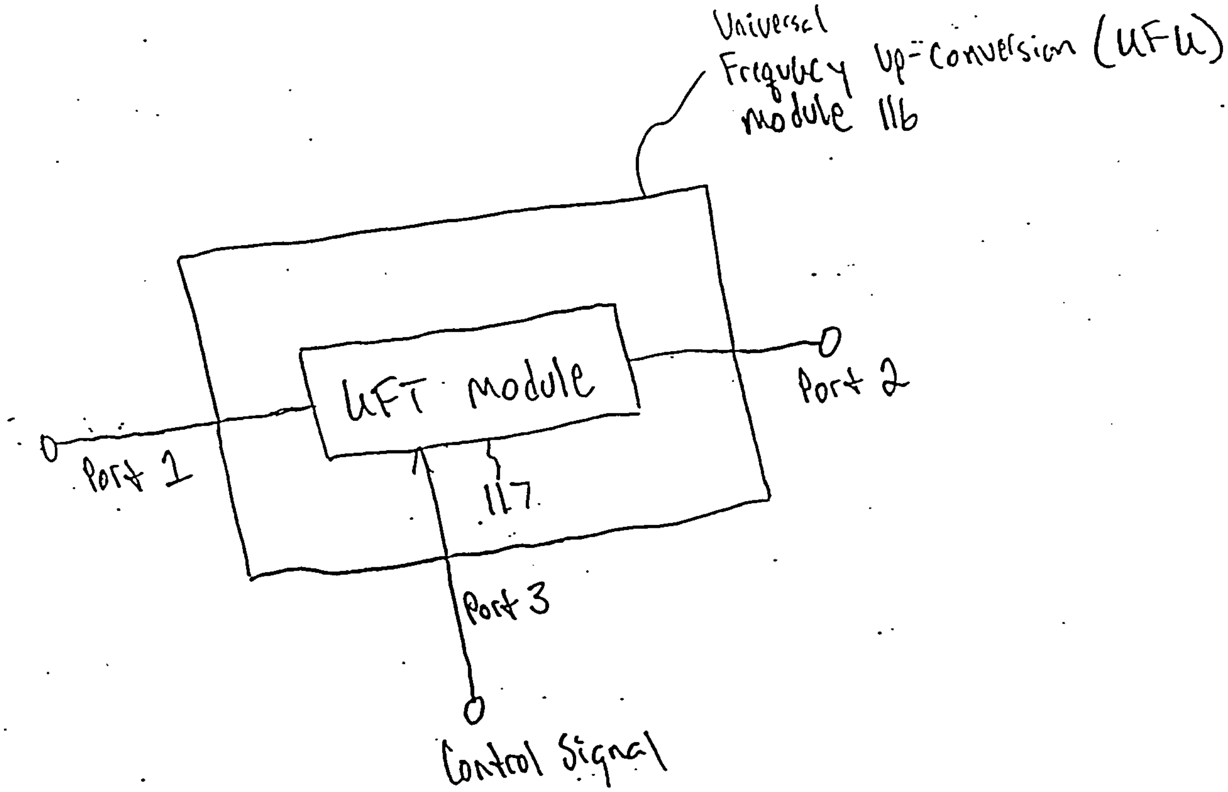
Universal Frequency Up-Conversion (UFU) module 116
UFT module
117
Port 1
Port 2
Port 3
Control Signal

FIG. 1D

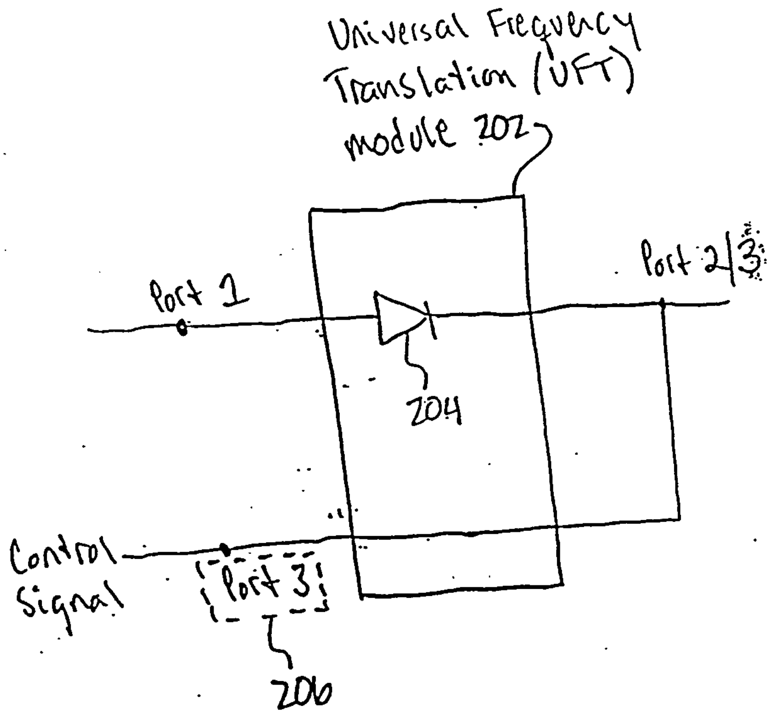
Universal Frequency Translation (UFT) module 202
Port 1
Port 2/3
204
Control Signal
Port 3
206

FIG. 2A

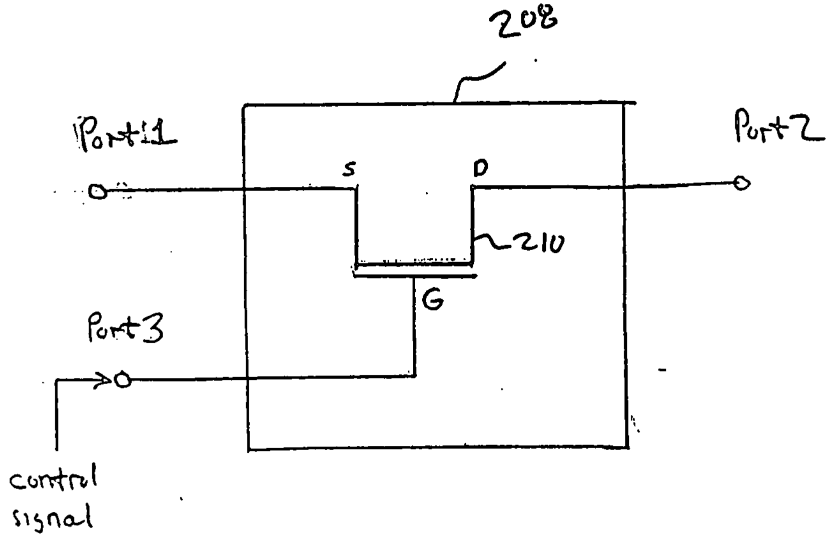

FIG. 2B

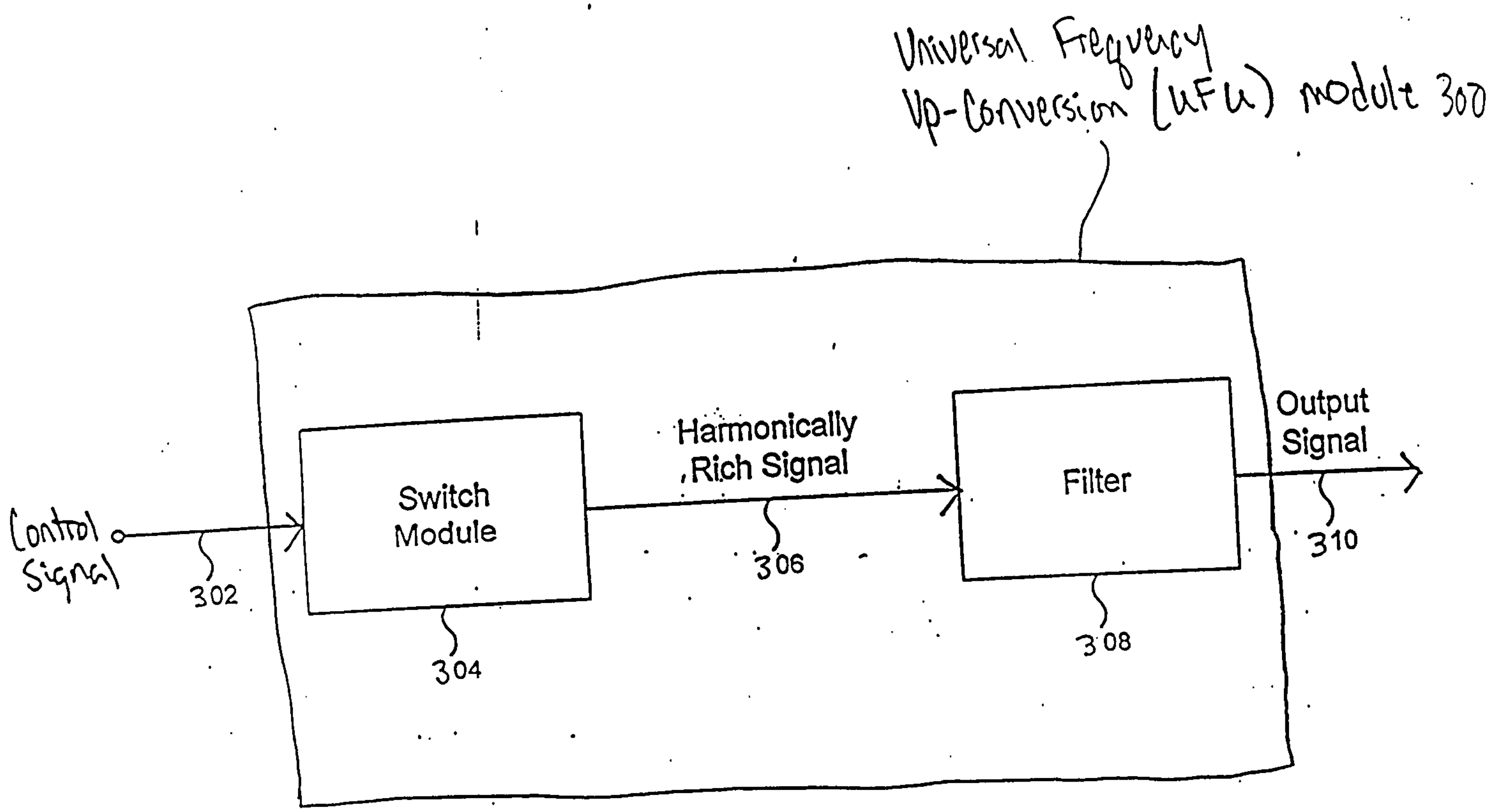

FIG. 3

9809-02.vsd/48

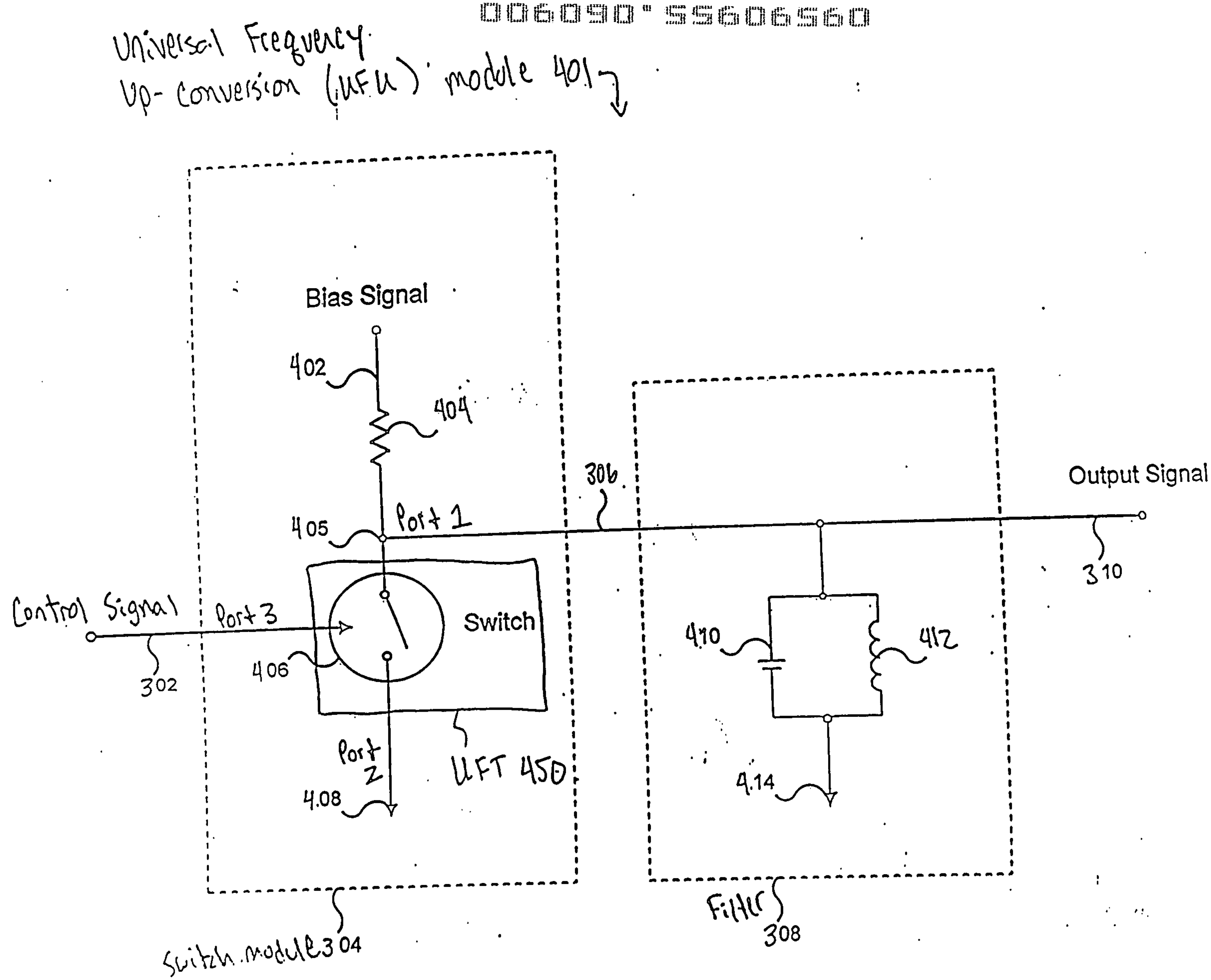

FIG. 4

9809-02.vsd/47

3

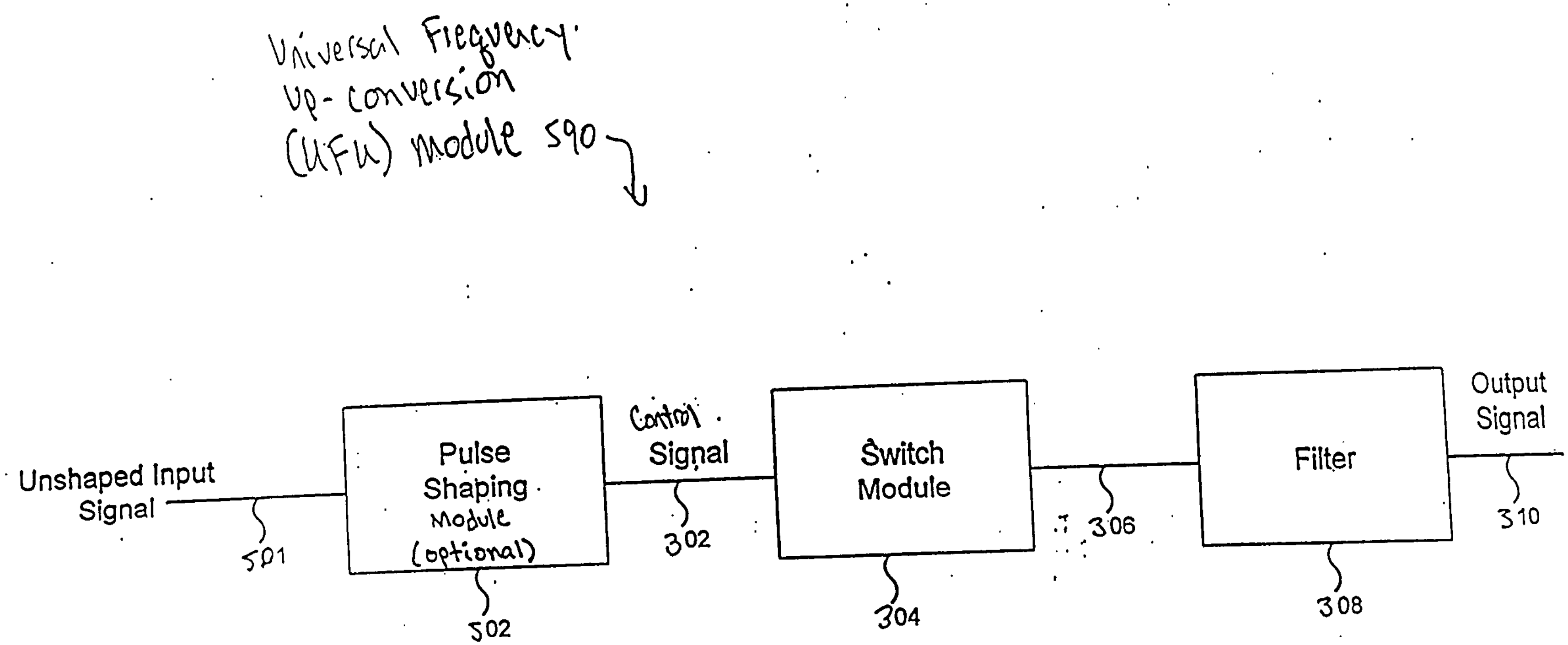

FIG. 5

9809-02.vsd/48

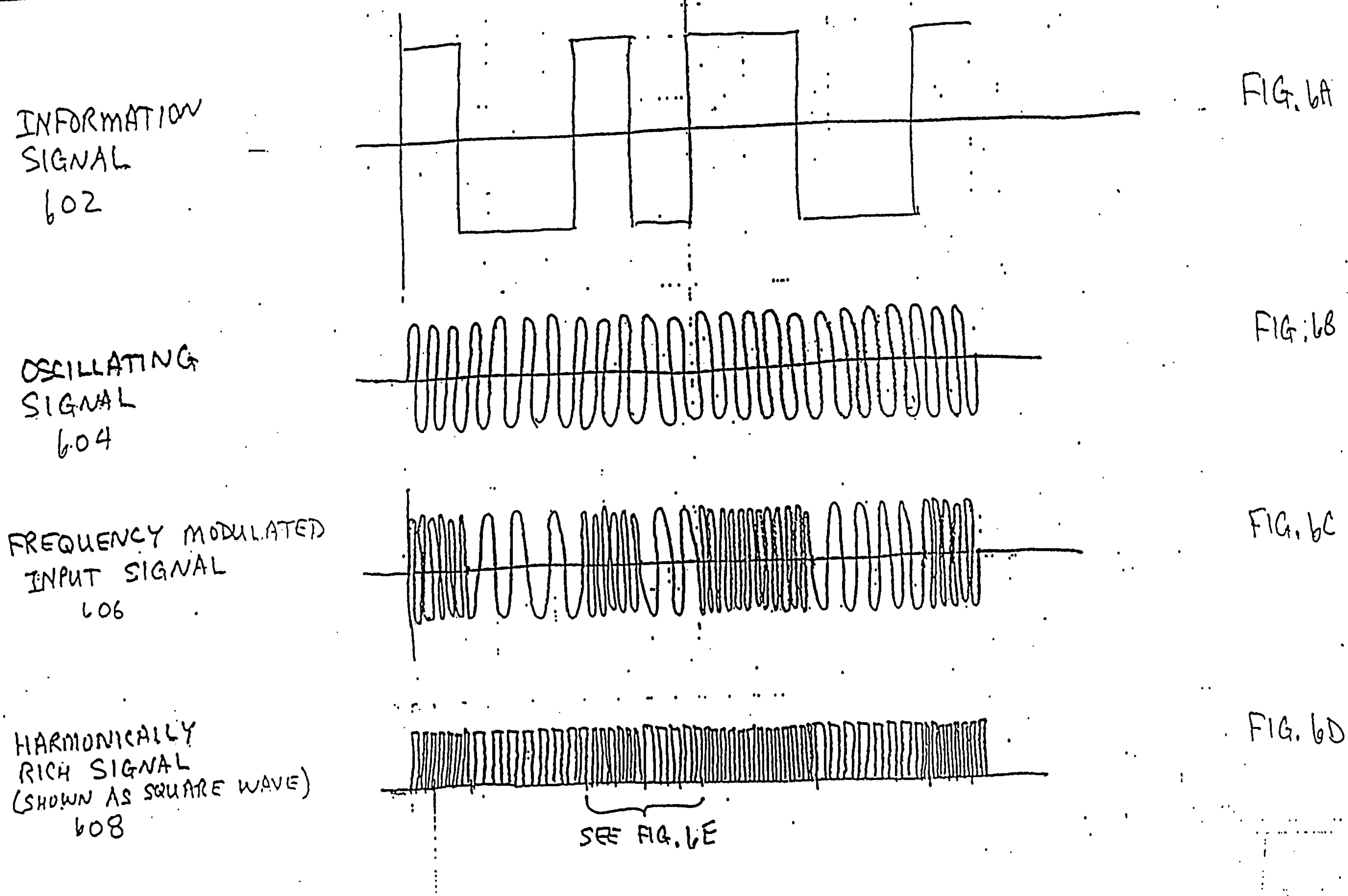
INFORMATION SIGNAL 602
FIG. 6A
OSCILLATING SIGNAL 604
FIG. 6B
FREQUENCY MODULATED INPUT SIGNAL 606
FIG. 6C
HARMONICALLY RICH SIGNAL (SHOWN AS SQUARE WAVE) 608
SEE FIG. 6E
FIG. 6D

FIG. 6

3

00609055606560

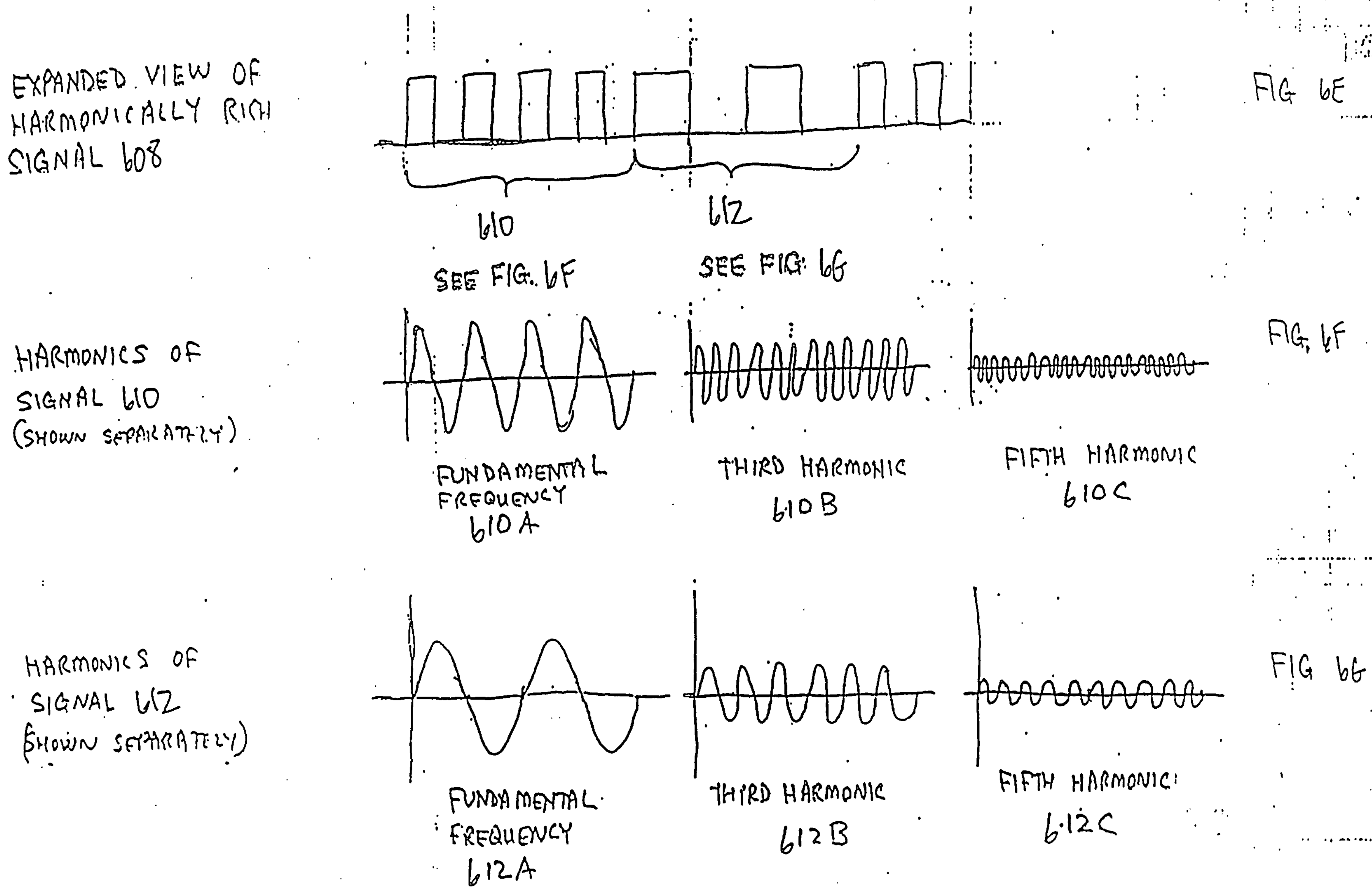

FIG. 6 (cont)

3

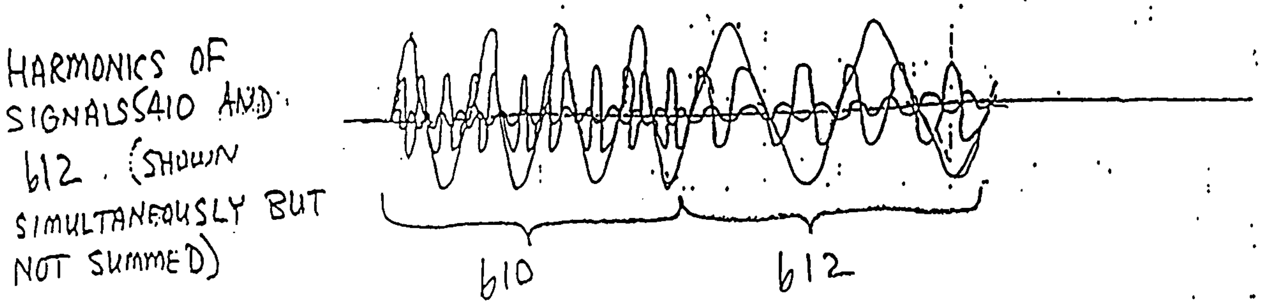

FIG 6H

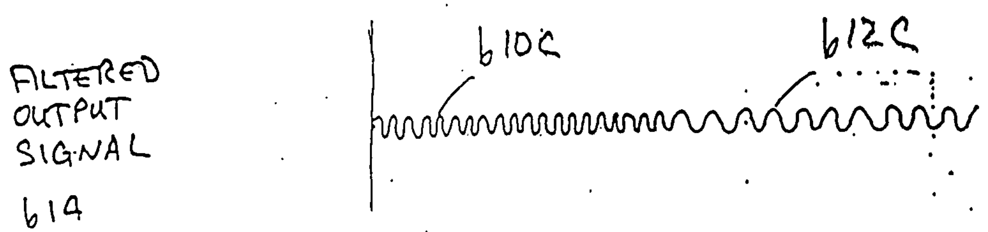

FIG. 6I

FIG 6 (cont.)

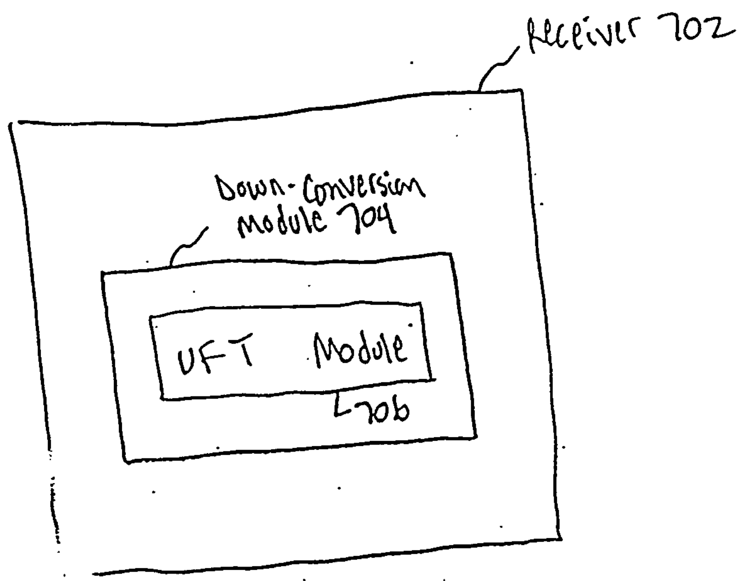

FIG. 7

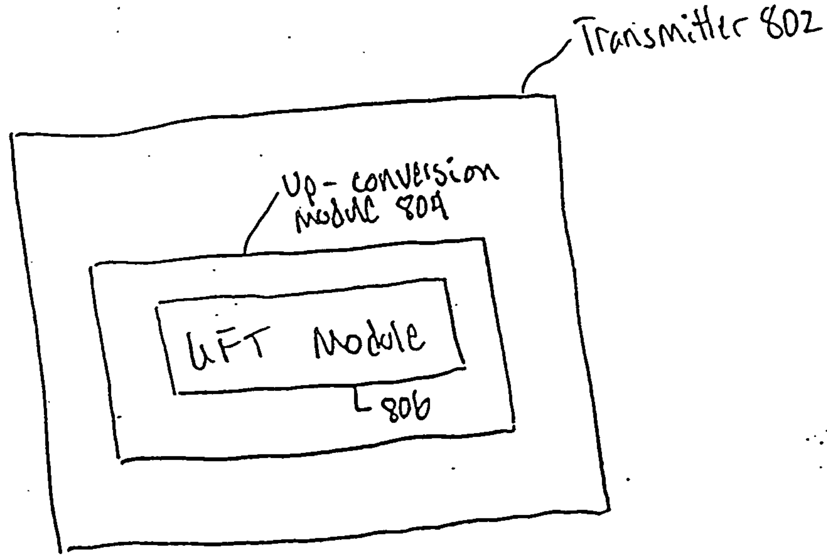

FIG. 8

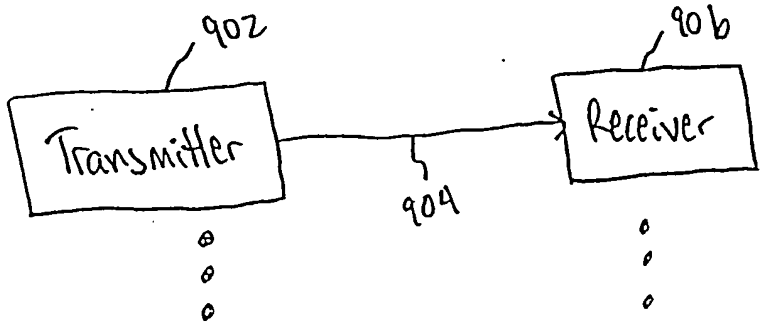

FIG. 9

m

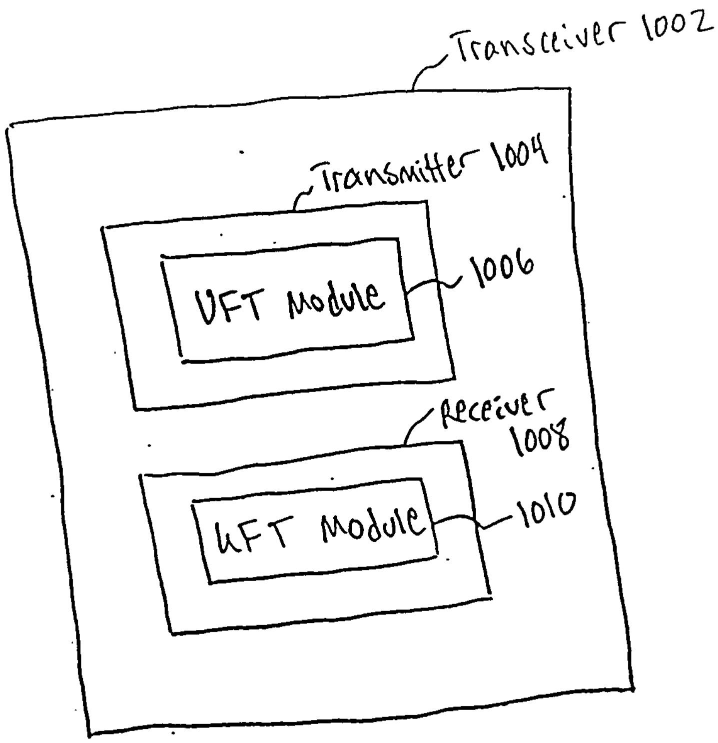
Transceiver 1002
Transmitter 1004
UFT Module
1006
Receiver 1008
UFT Module
1010

FIG. 10

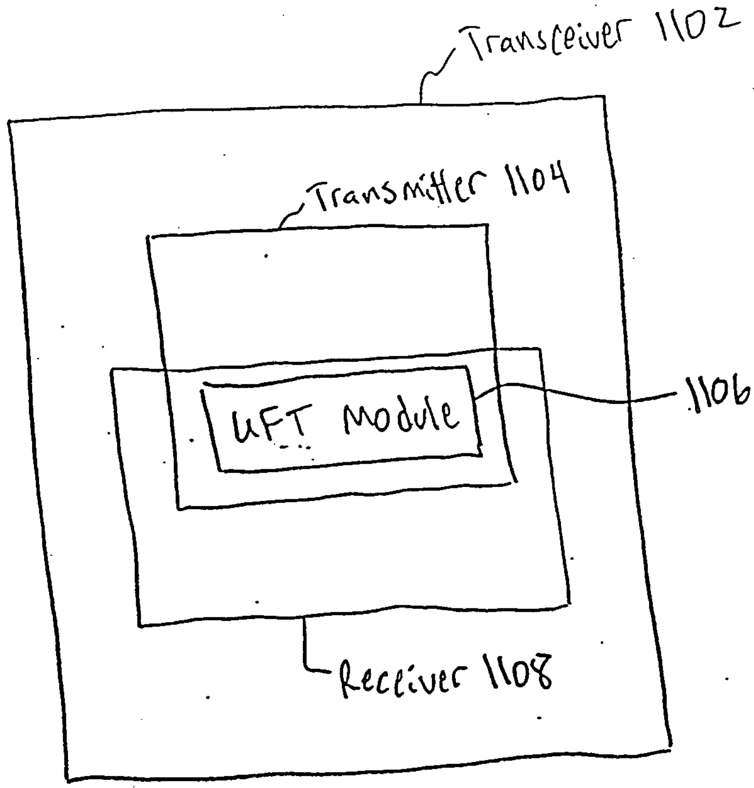
Transceiver 1102
Transmitter 1104
UFT Module
1106
Receiver 1108

FIG. 11

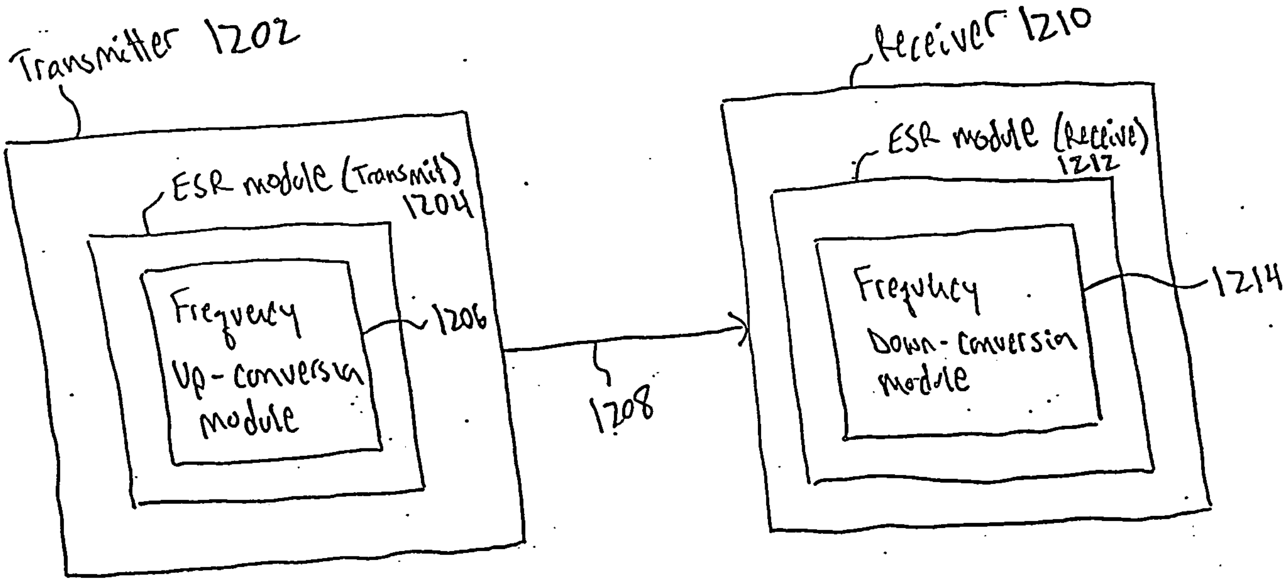
Transmitter 1202
ESR module (Transmit) 1204
Frequency Up-conversion module
1206
1208
Receiver 1210
ESR module (Receive) 1212
Frequency Down-conversion module
1214

FIG. 12

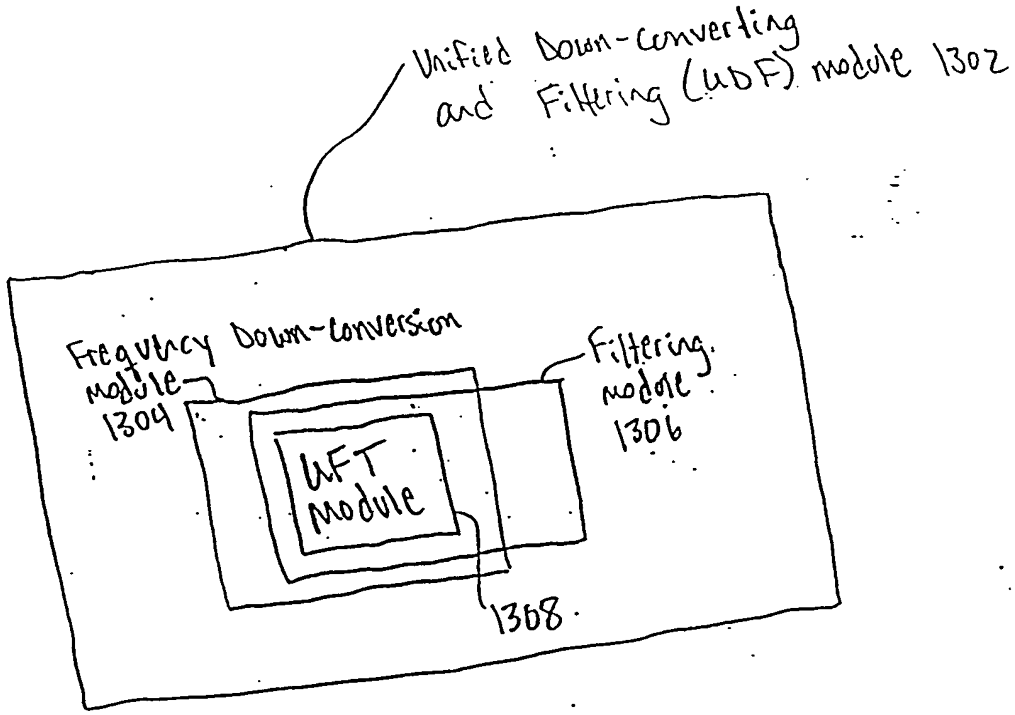
Unified Down-converting and Filtering (UDF) module 1302
Frequency Down-conversion module 1304
Filtering module 1306
UFT Module
1308

FIG. 13

m

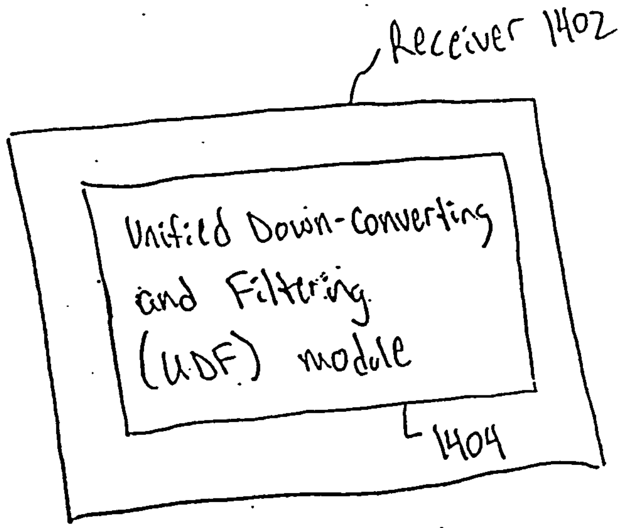
Receiver 1402
Unified Down-Converting and Filtering (UDF) module
1404

FIG. 14

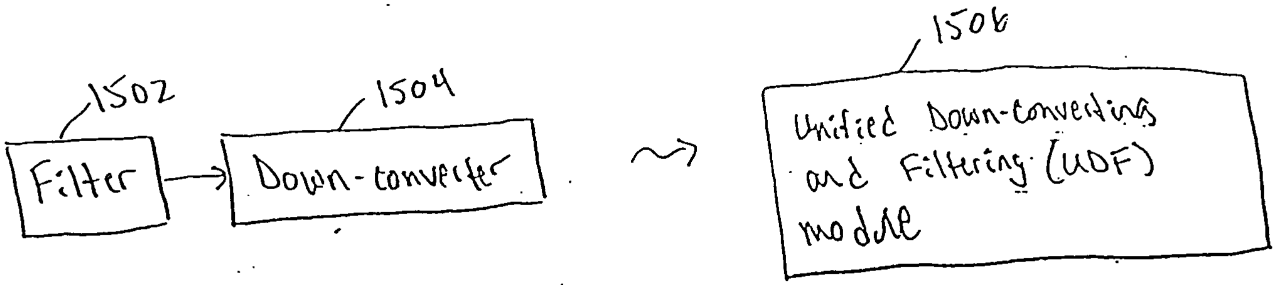

FIG. 15A

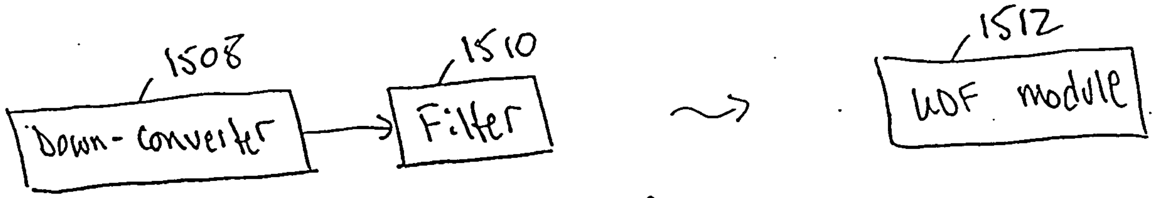

FIG. 15B

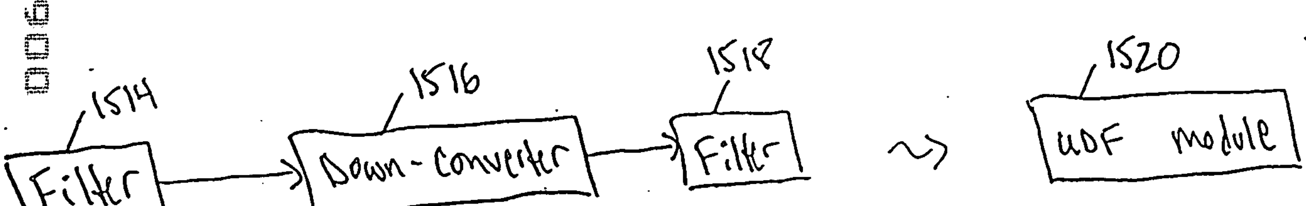

FIG. 15C

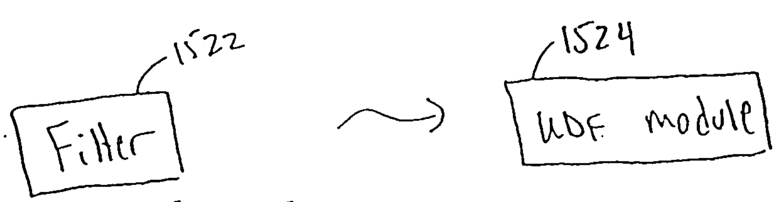

FIG. 15D

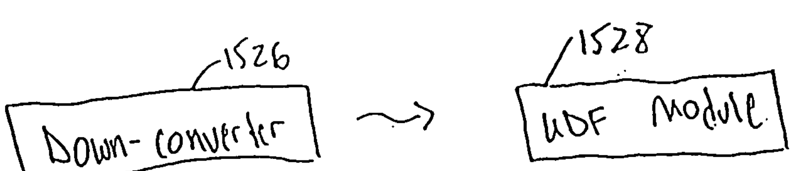

FIG. 15E

m

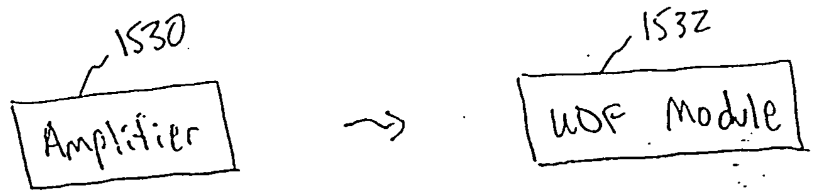

FIG. 15F

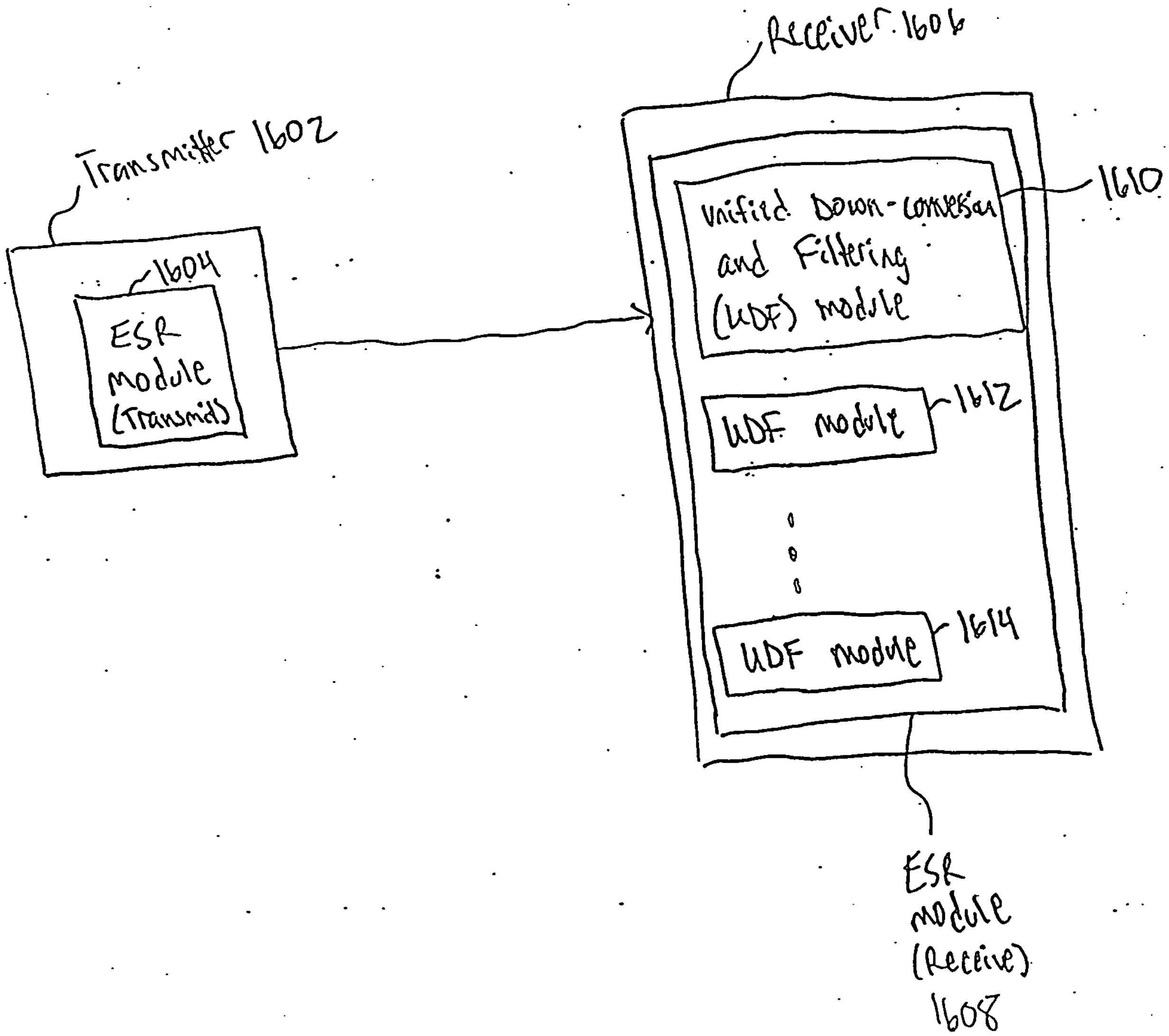

FIG. 16

0060090 "55605560

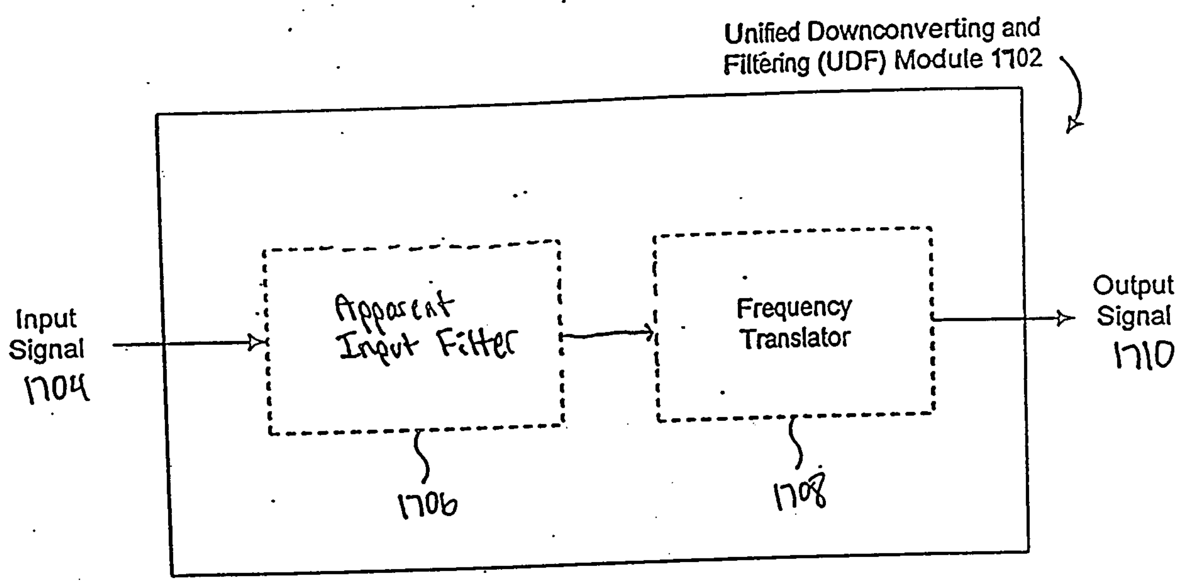

FIG. 17

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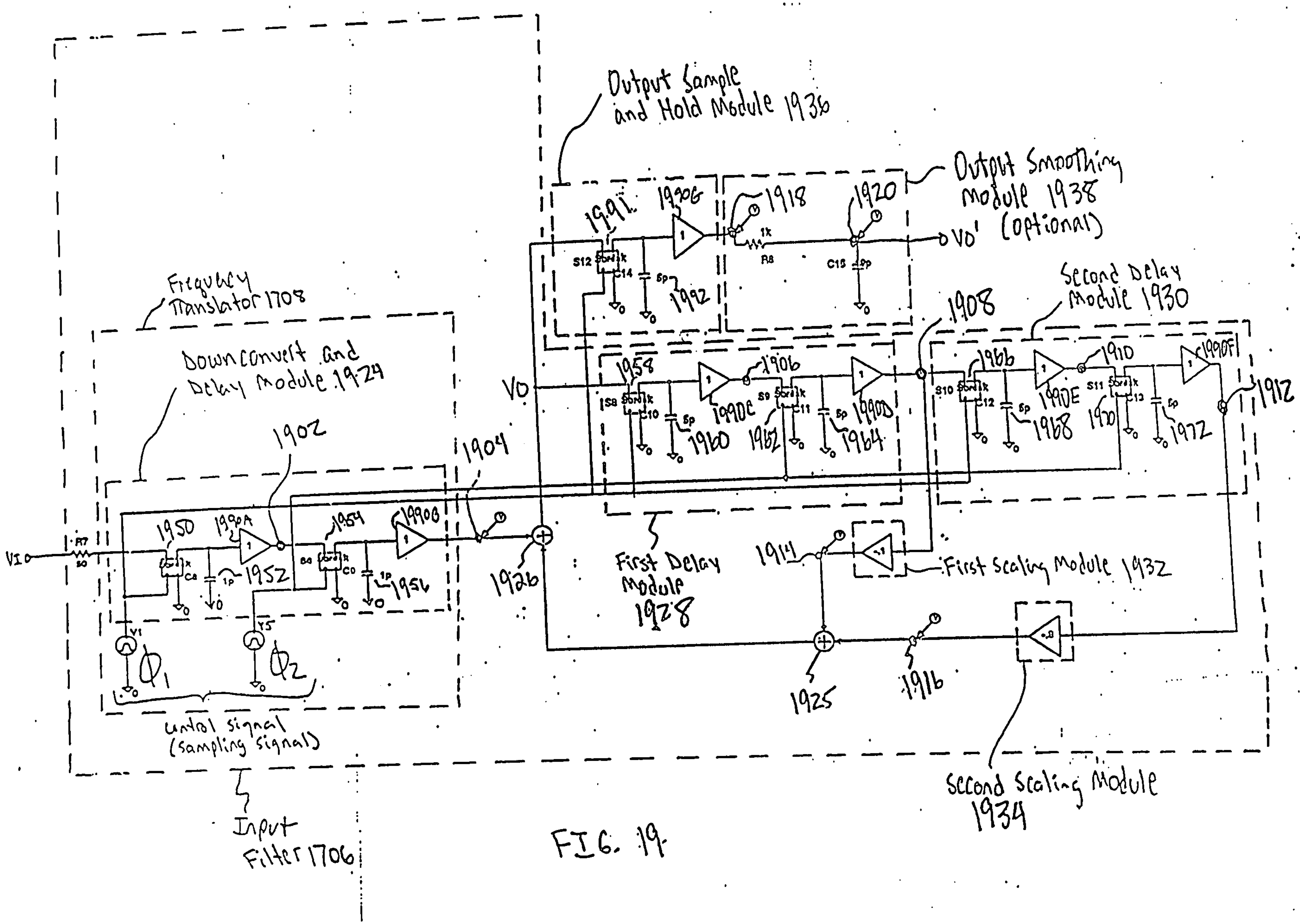
9809-02.vsd/13

1802

Time / Node	t-1 (rising edge of ϕ_1)	t-1 (rising edge of ϕ_2)	t (rising edge of ϕ_1)	t (rising edge of ϕ_2)	t+1 (rising edge of ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	$VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$ 1850

FIG. 18



VDF Module 1922 (band pass)
Output Sample and Hold Module 1936
Output Smoothing Module 1938 (optional)
Frequency Translator 1708
Down convert and Delay Module 1924
Second Delay Module 1930
First Delay Module 1928
First Scaling Module 1932
Second Scaling Module 1934
Control signal (sampling signal)
Input Filter 1706
VI
VO
VO'
1902
1904
1906
1908
1910
1912
1914
1916
1918
1920
1925
1926
1950
1952
1954
1956
1958
1960
1962
1964
1966
1968
1970
1972
1990A
1990B
1990C
1990D
1990E
1990F
1990G
1991
1992

FIG. 19

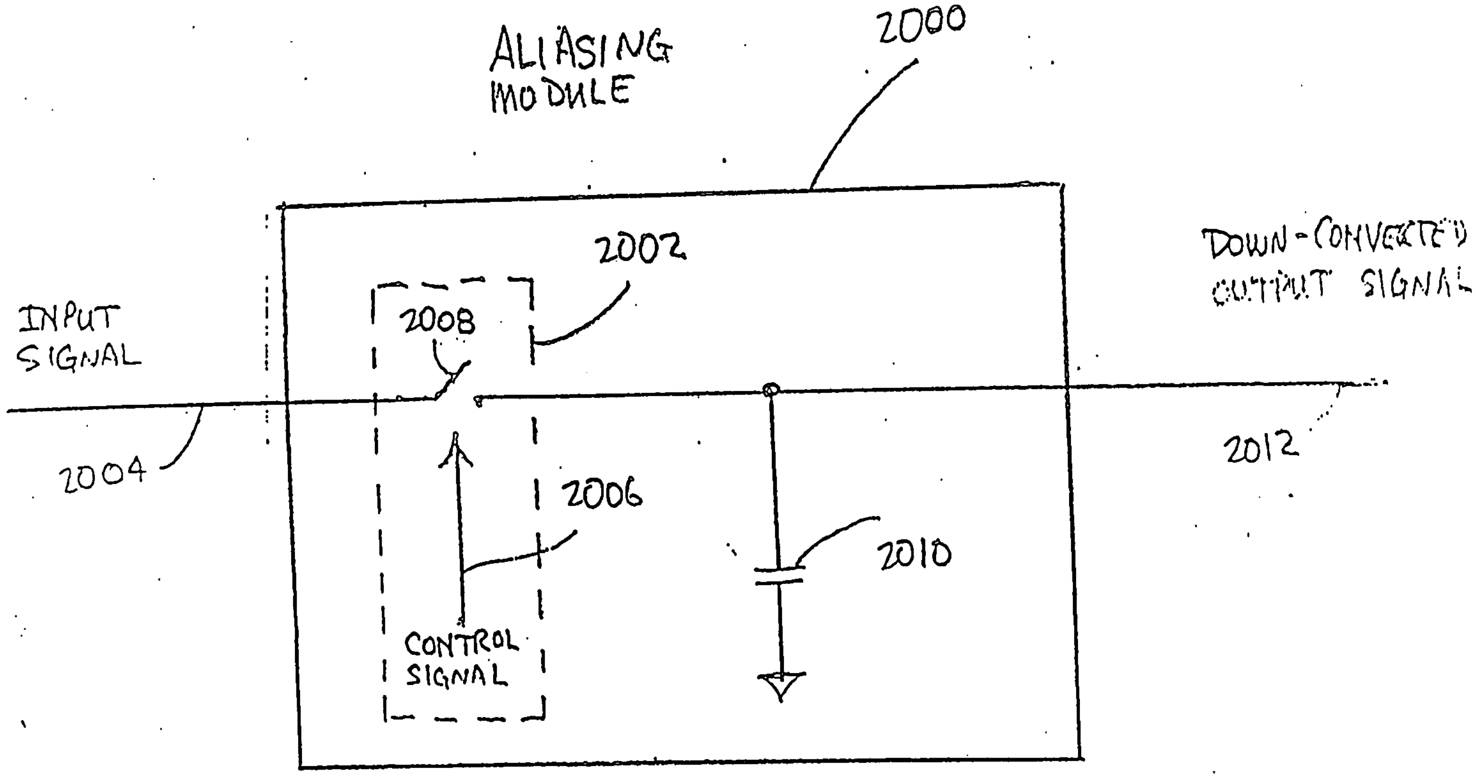

ALIASING MODULE
2000
2002
2008
INPUT SIGNAL
2004
2006
CONTROL SIGNAL
2010
DOWN-CONVERTED OUTPUT SIGNAL
2012

FIG. 20A

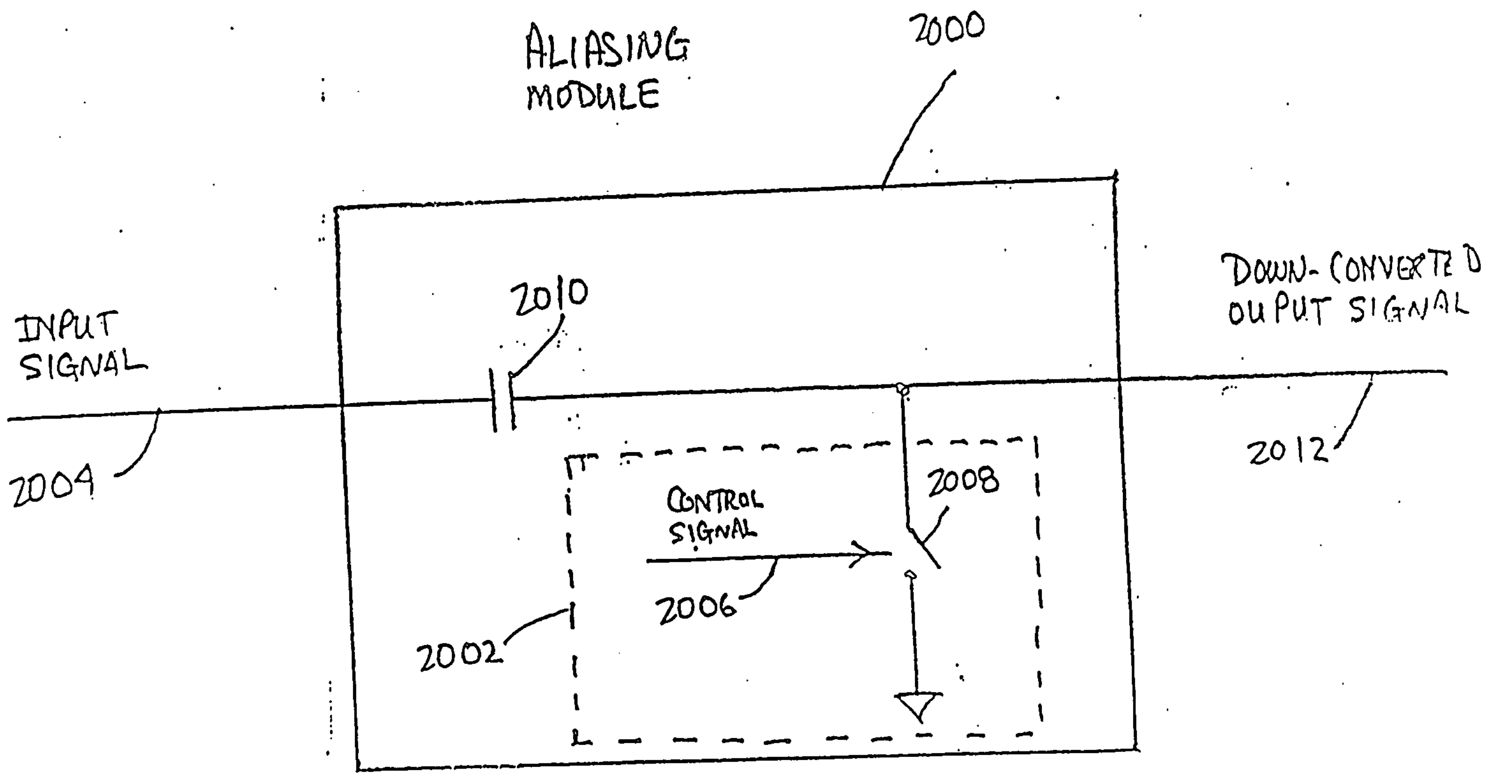

ALIASING
MODULE
2000
INPUT
SIGNAL
2004
2010
DOWN-CONVERTED
OUPUT SIGNAL
2012
2008
CONTROL
SIGNAL
2006
2002

FIG. 20A-1

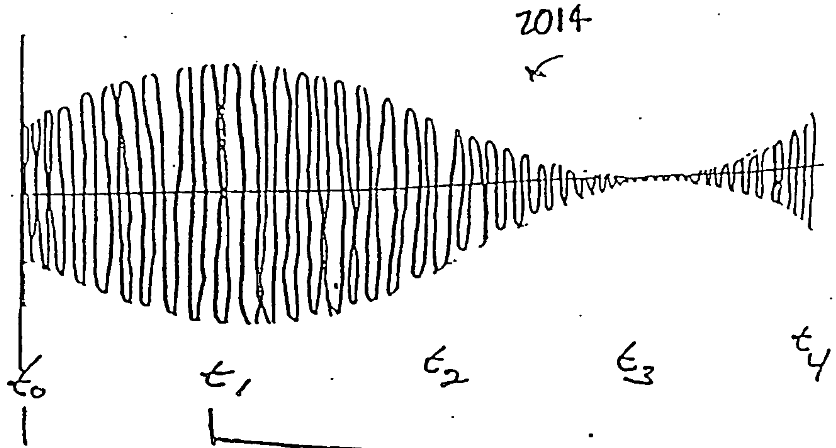


FIG. 20B

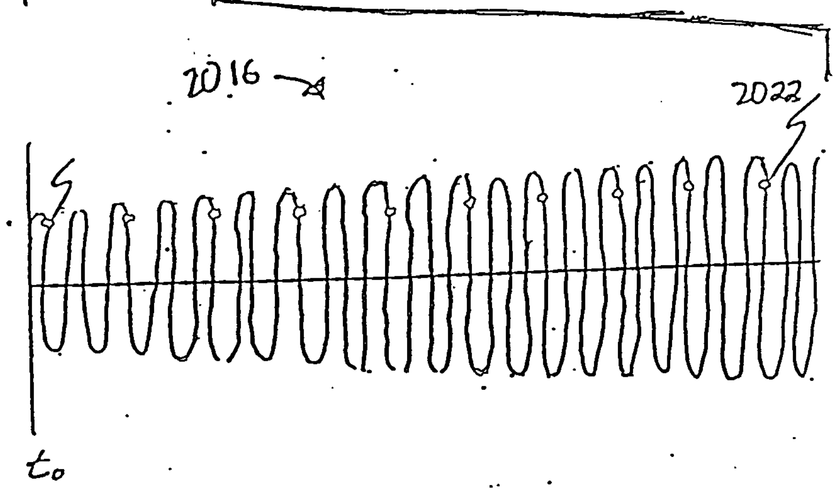


FIG. 20C

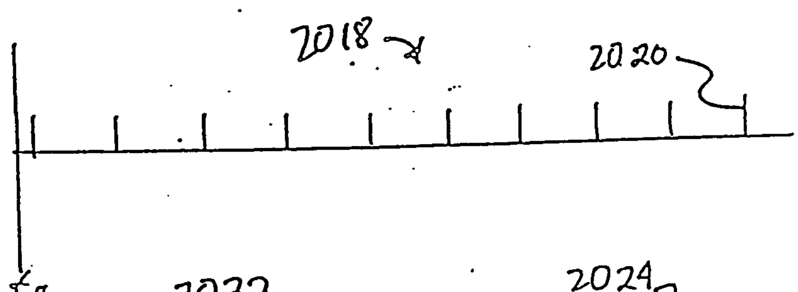


FIG. 20D

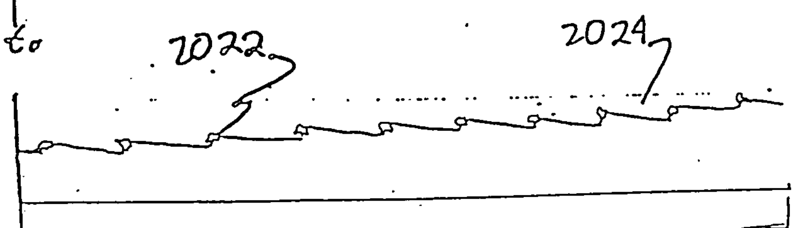


FIG. 20E

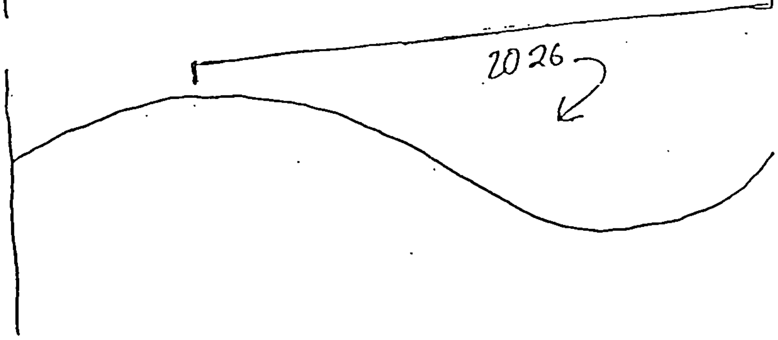


FIG. 20F

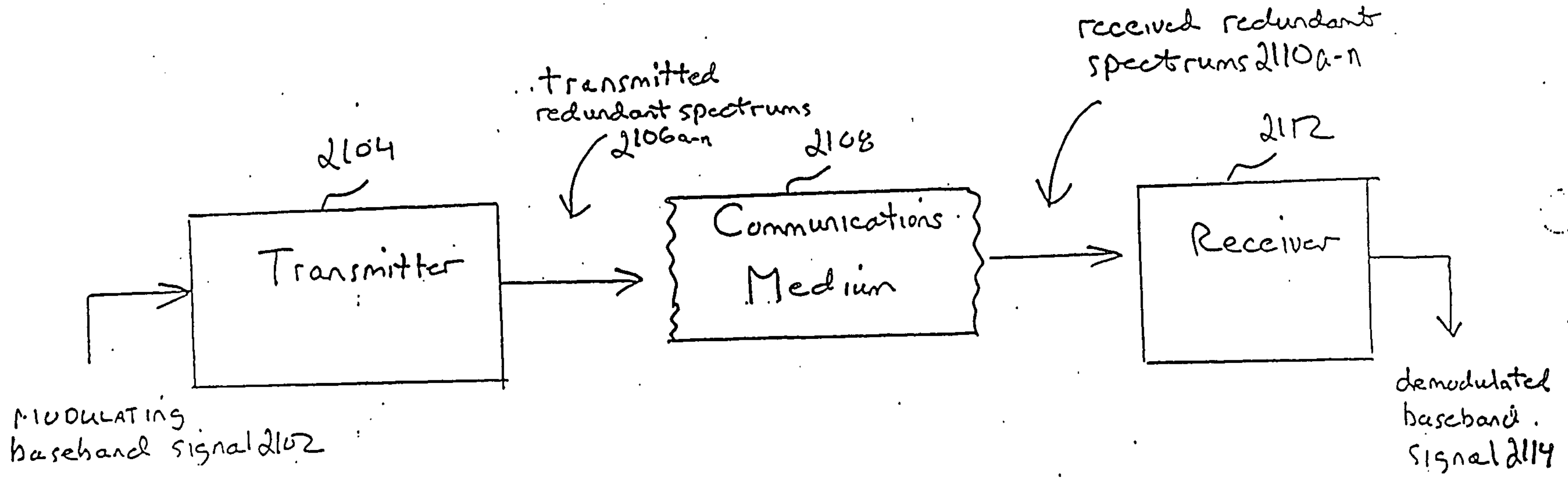

transmitted
redundant spectrums
2106a-n
received redundant
spectrums 2110a-n
2104
2108
2112
Transmitter
Communications
Medium
Receiver
MODULATING
baseband signal 2102
demodulated
baseband
signal 2114

FIG. 21

FIG. 22A

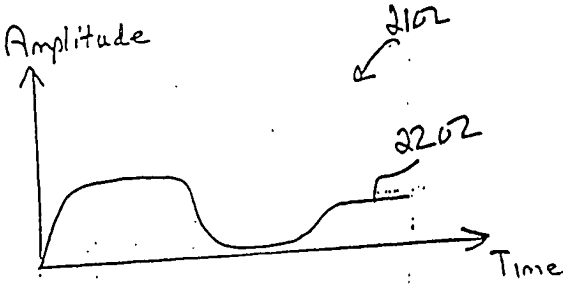


FIG. 22B

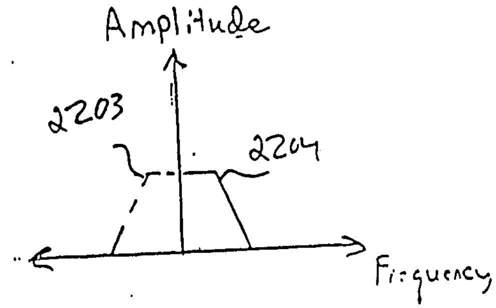


FIG. 22C

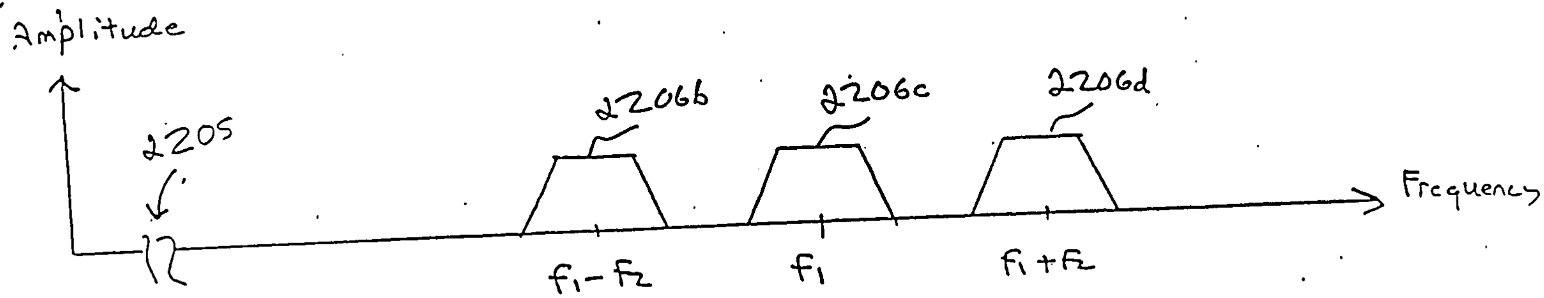


FIG. 22D

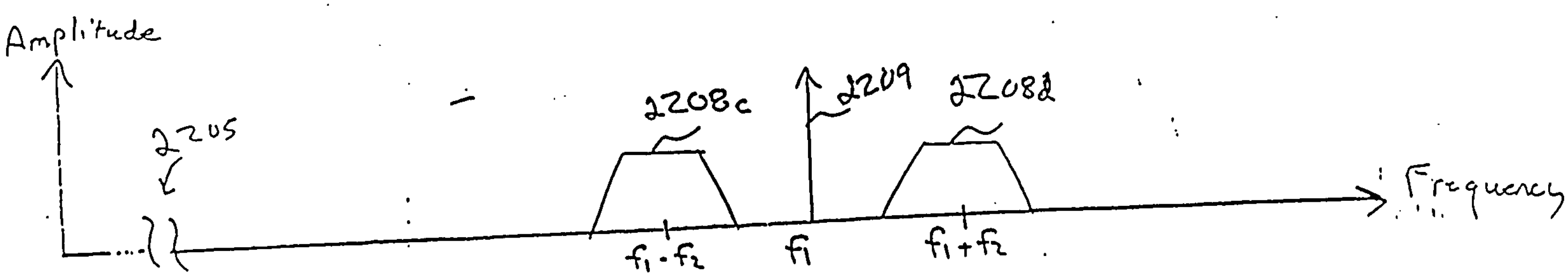


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FIG. 22E

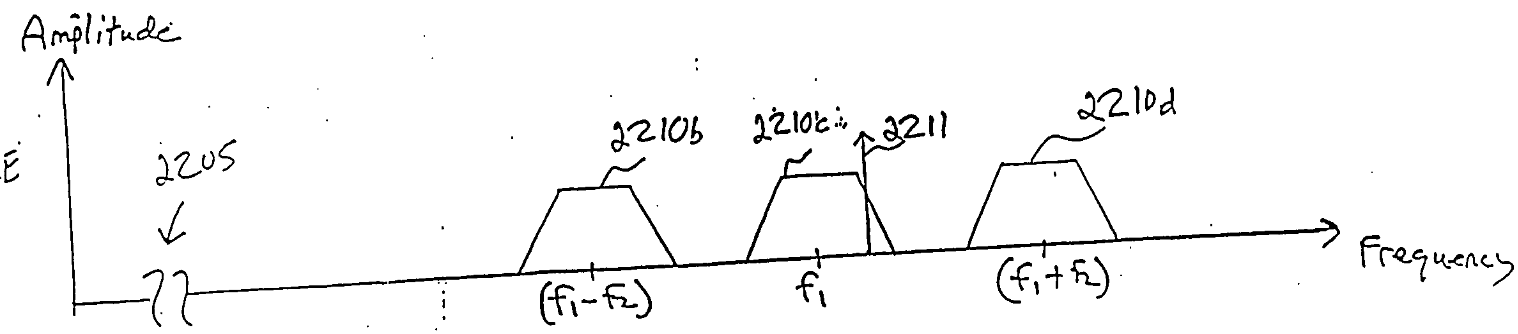


FIG. 22F

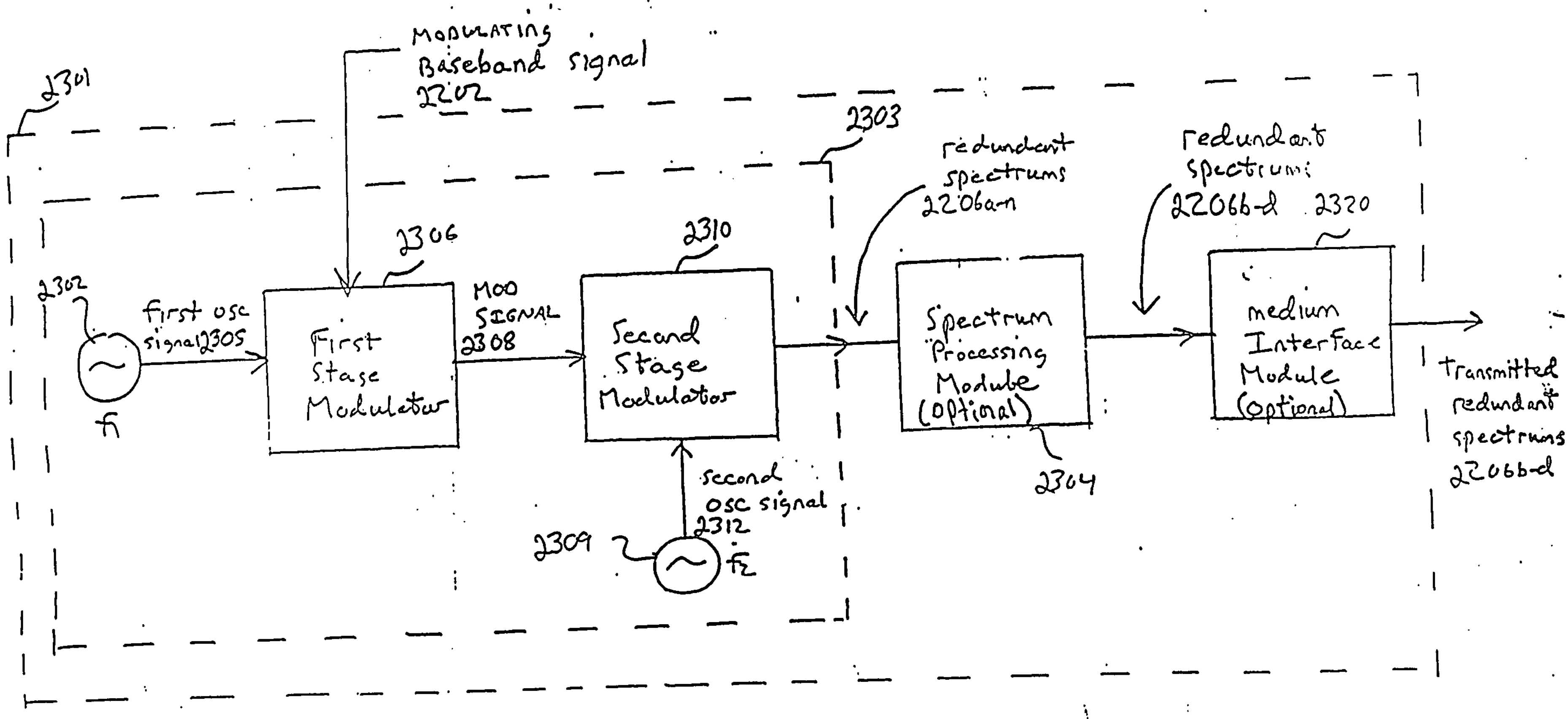

MODULATING Baseband signal 2202
2301
2303
redundant spectrums 2206a-n
redundant spectrum: 2206b-d
2320
2306
2310
2302
first osc signal 2305
First Stage Modulator
MOD SIGNAL 2308
Second Stage Modulator
Spectrum Processing Module (optional)
medium Interface Module (optional)
Transmitted redundant spectrums 2206b-d
f1
2304
second osc signal 2312
2309
f2

FIG. 23A

FIG. 23B

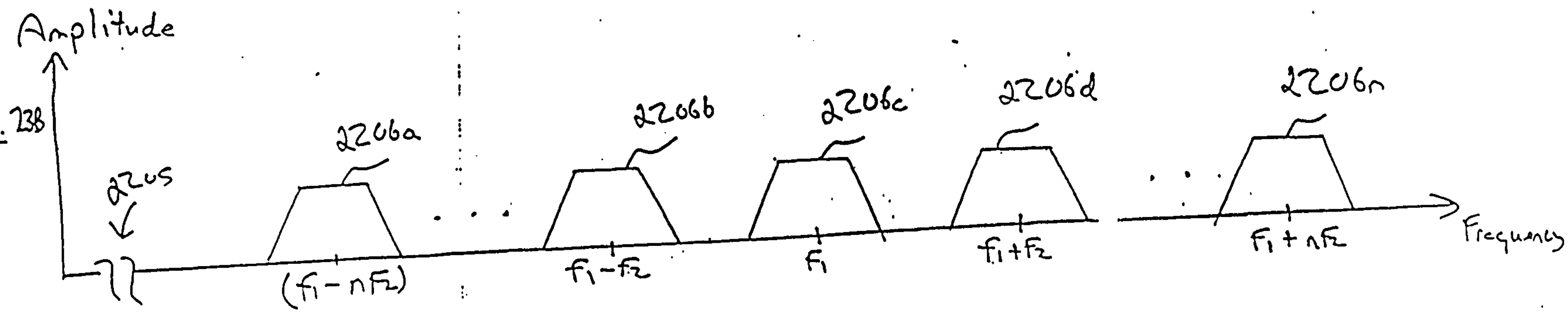
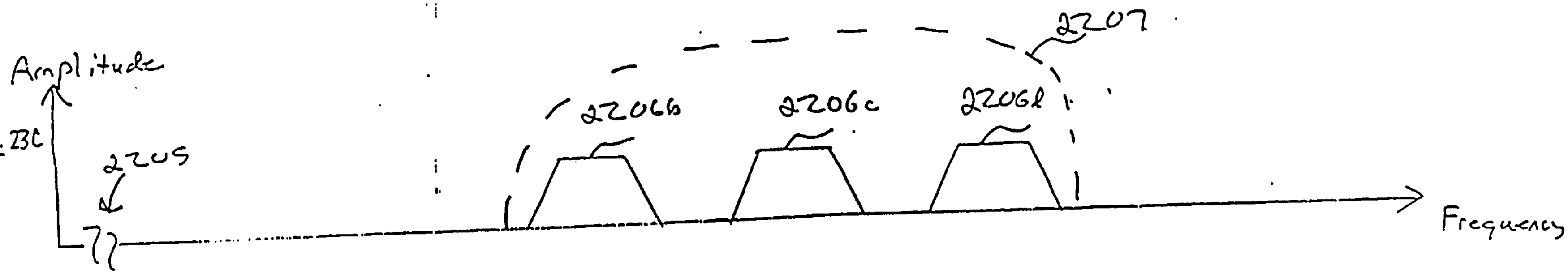


FIG. 23C



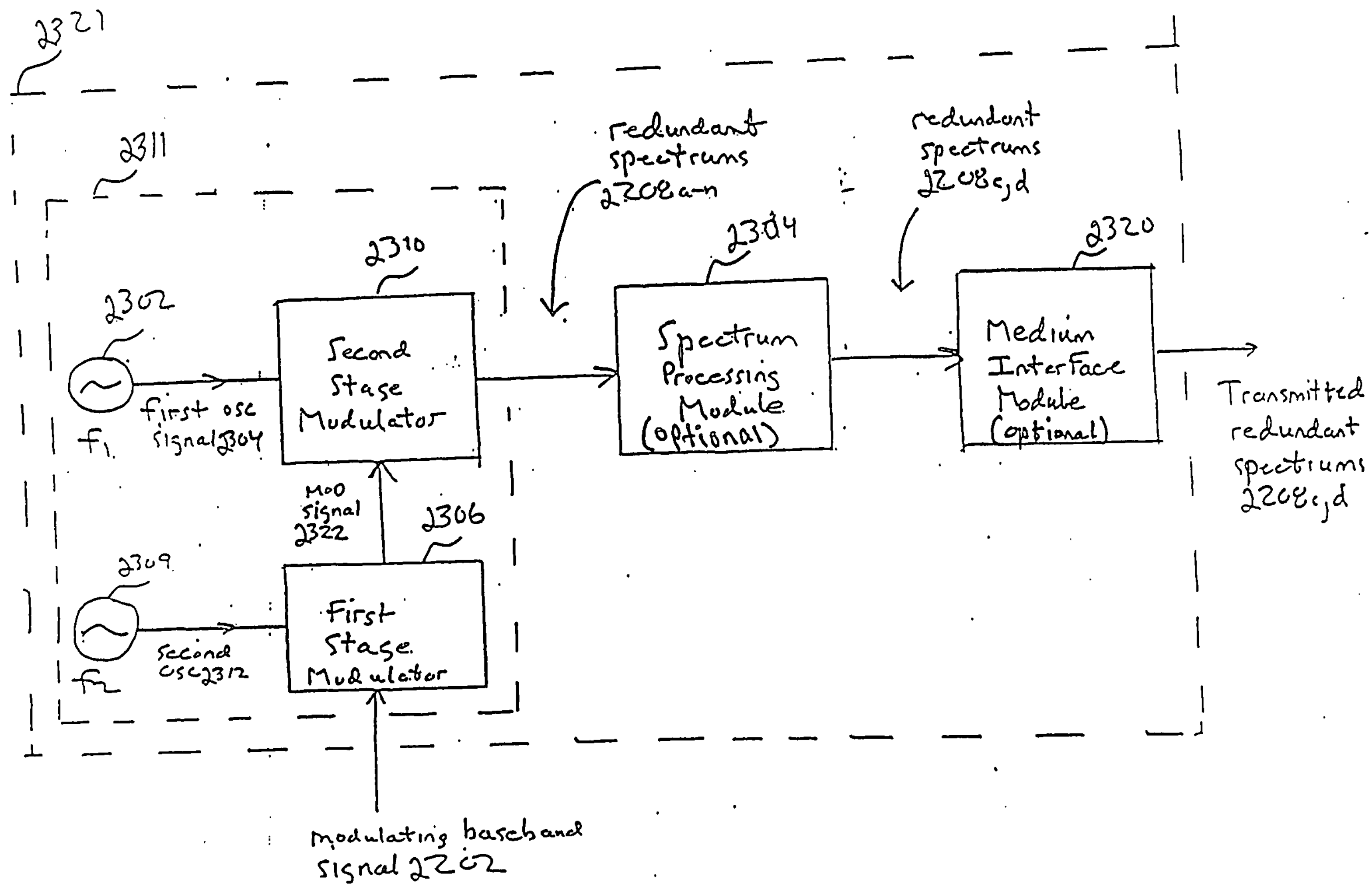

2321
2311
2302
f1
first osc signal 2304
2309
f2
second osc 2312
2310
Second Stage Modulator
MOO signal 2322
2306
First Stage Modulator
modulating baseband signal 2202
redundant spectrums 2208a-n
2304
Spectrum Processing Module (optional)
redundant spectrums 2208c,d
2320
Medium Interface Module (optional)
Transmitted redundant spectrums 2208c,d

FIG. 23D

FIG. 23E

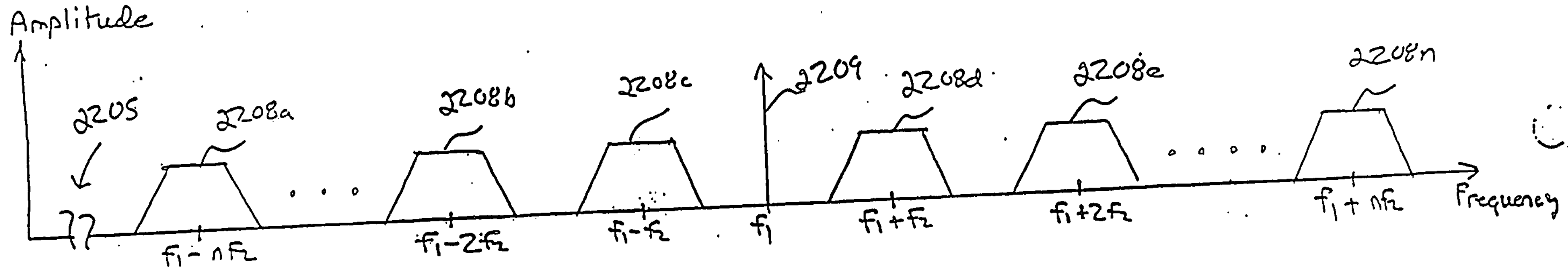
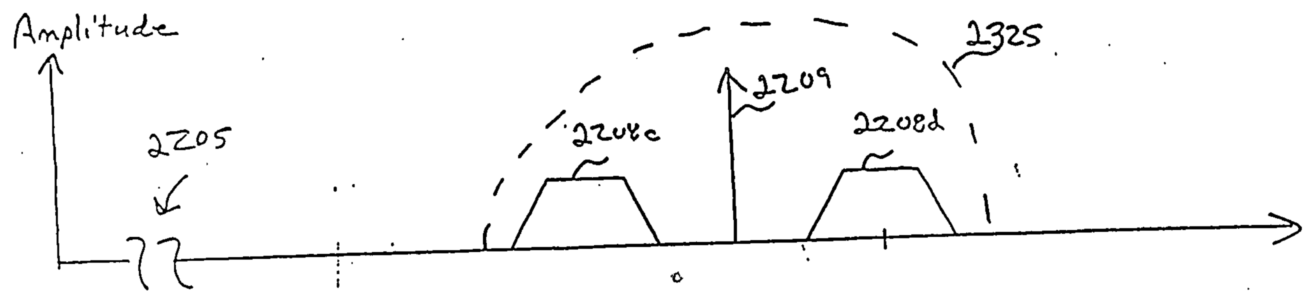


FIG. 23F



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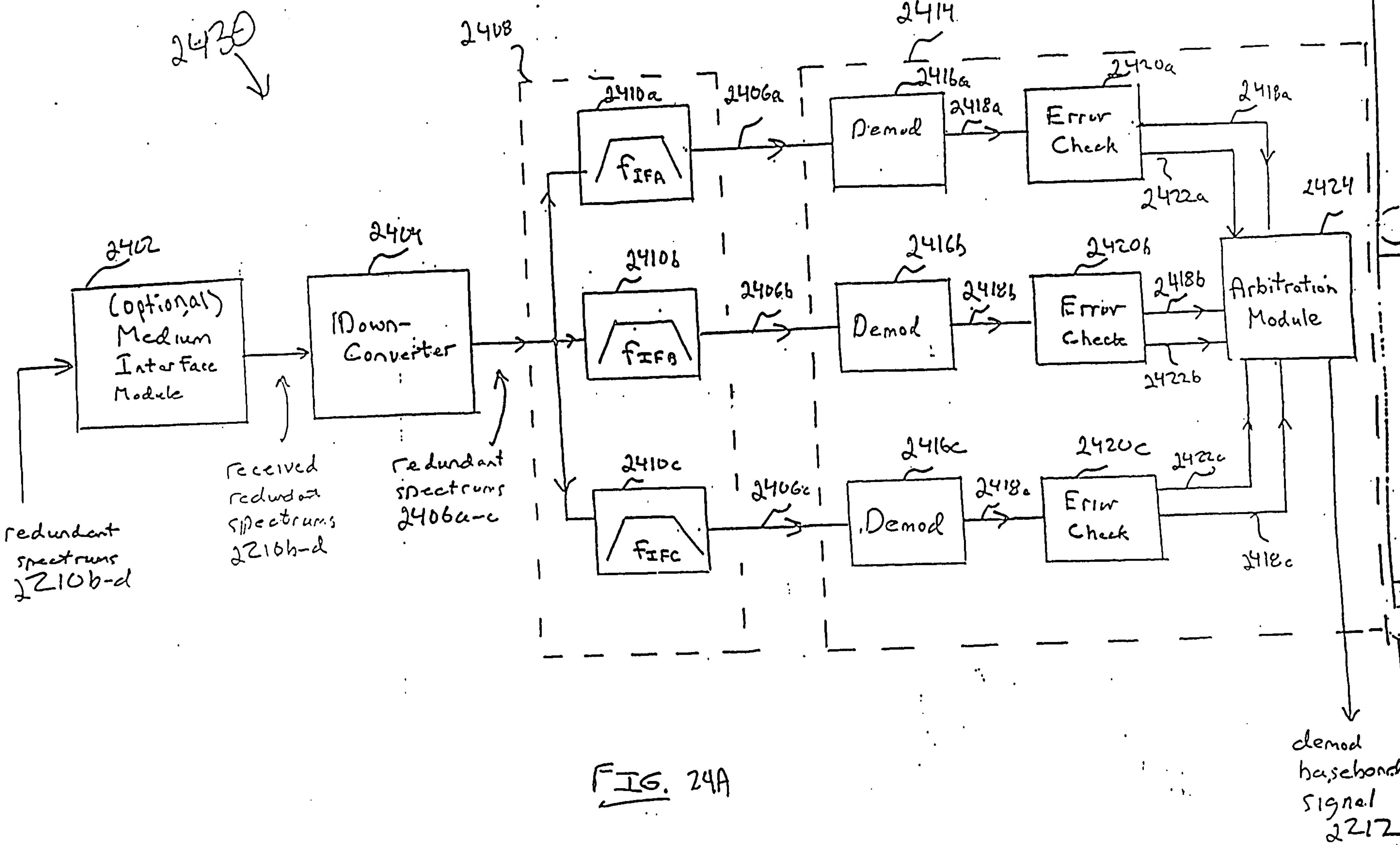


FIG. 24A

FIG. 24B

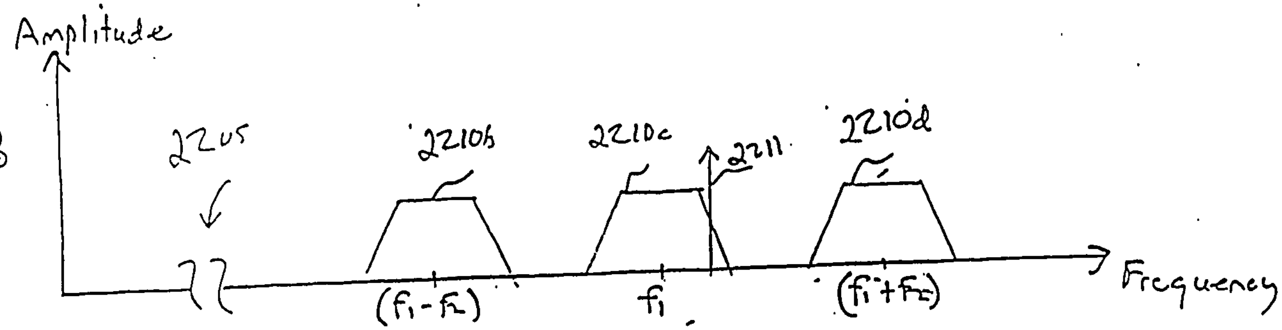


FIG. 24C.

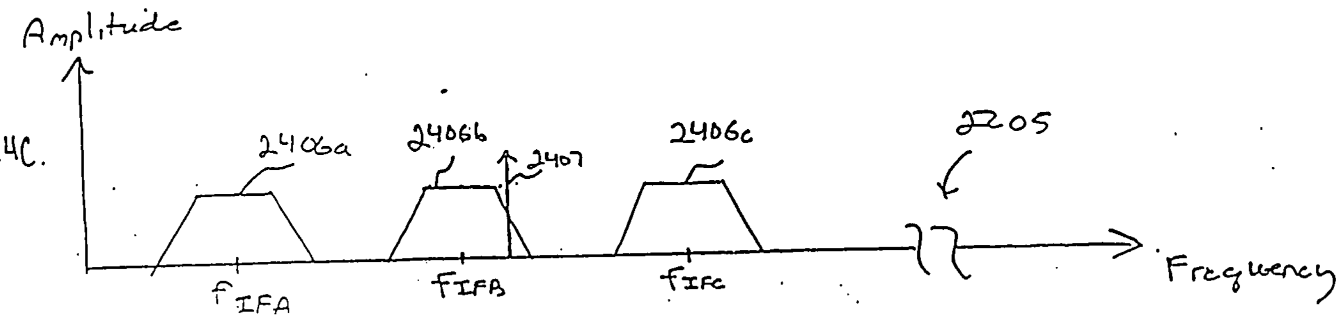


FIG. 24D

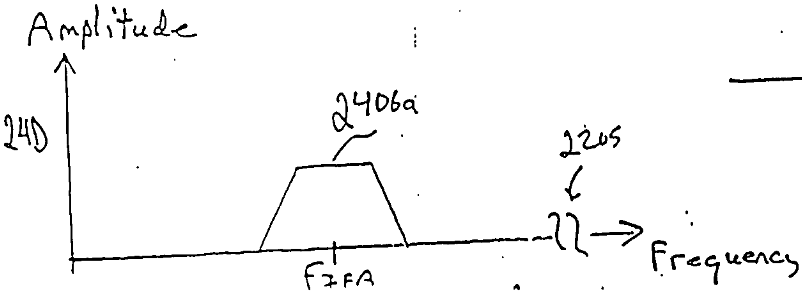


FIG. 24G

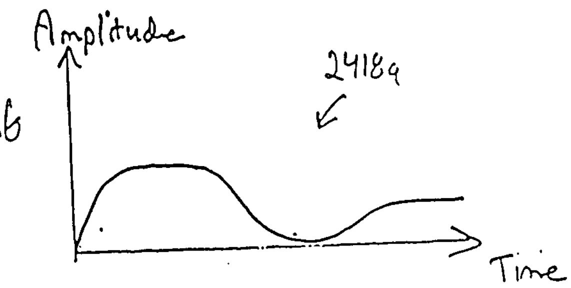


FIG. 24E

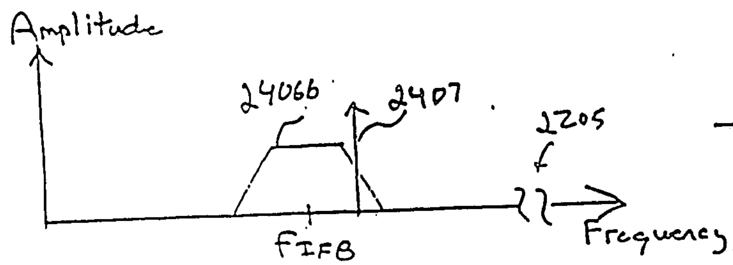


FIG. 24H

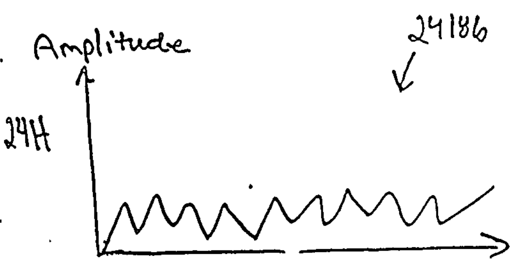


FIG 24F

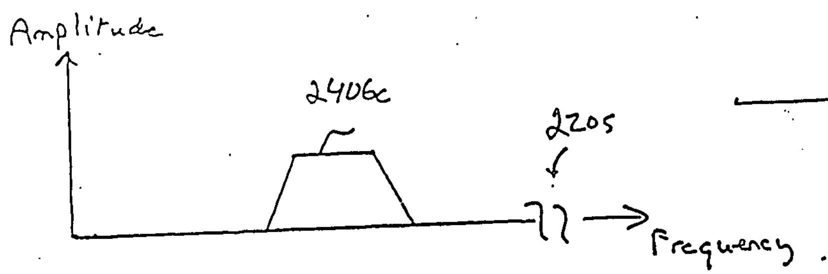
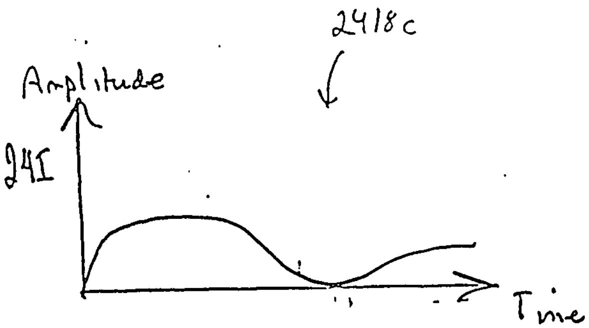


FIG. 24I



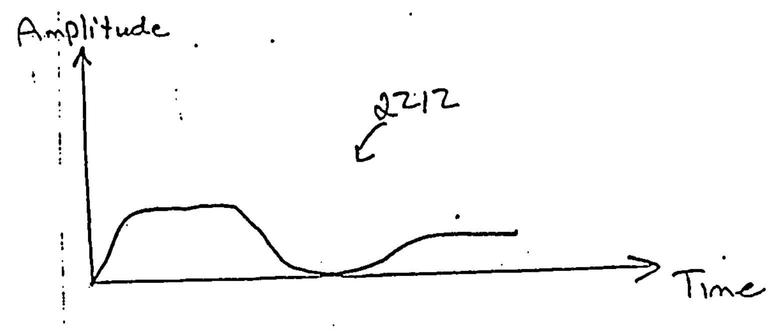


FIG. 24J

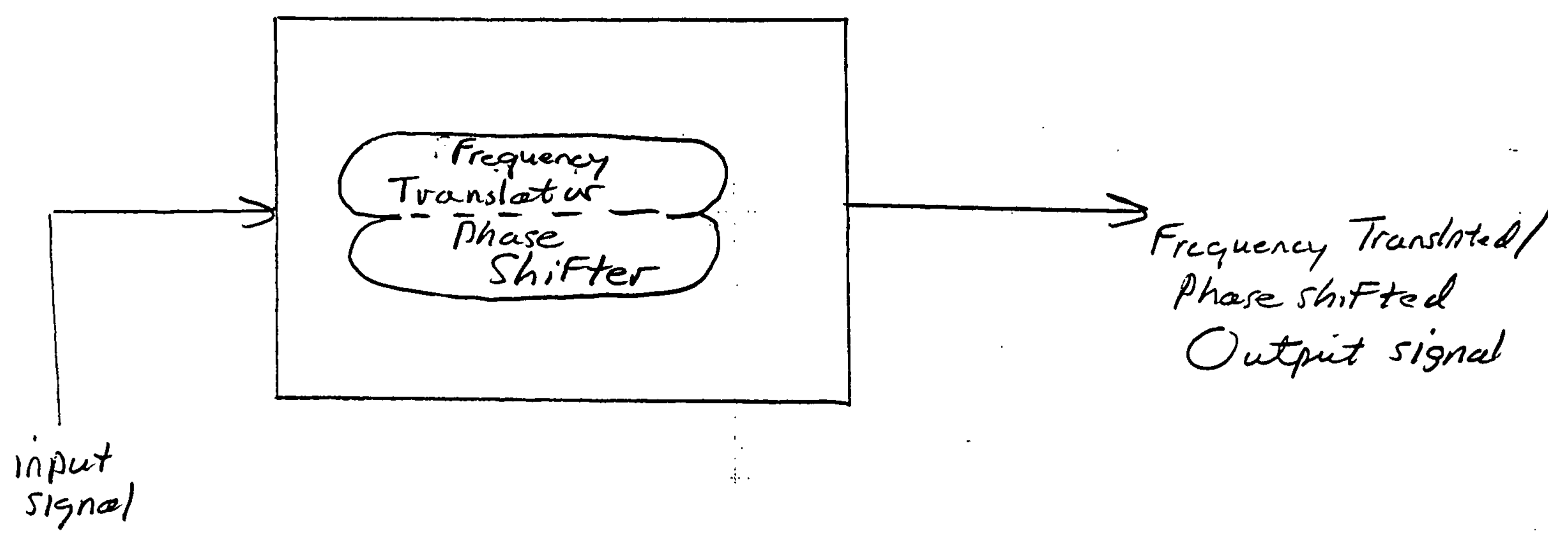

Frequency Translator
Phase Shifter
input signal
Frequency Translated/
Phase shifted
Output signal

FIG. 25A

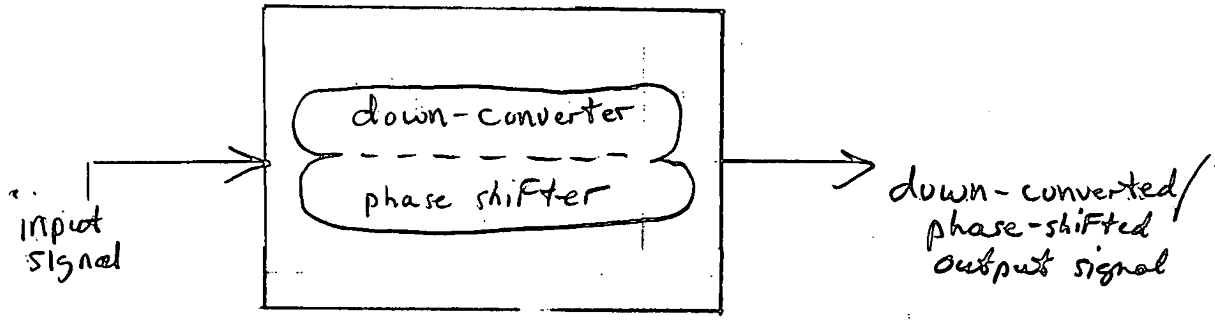


FIG. 25B

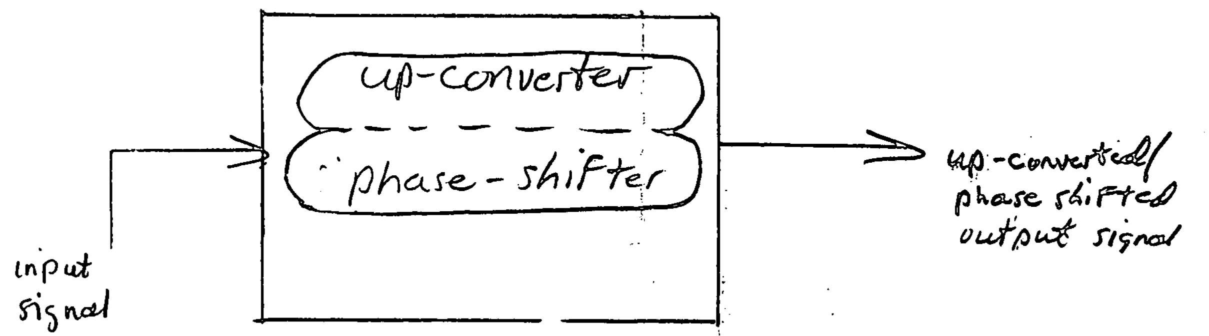


FIG. 25C

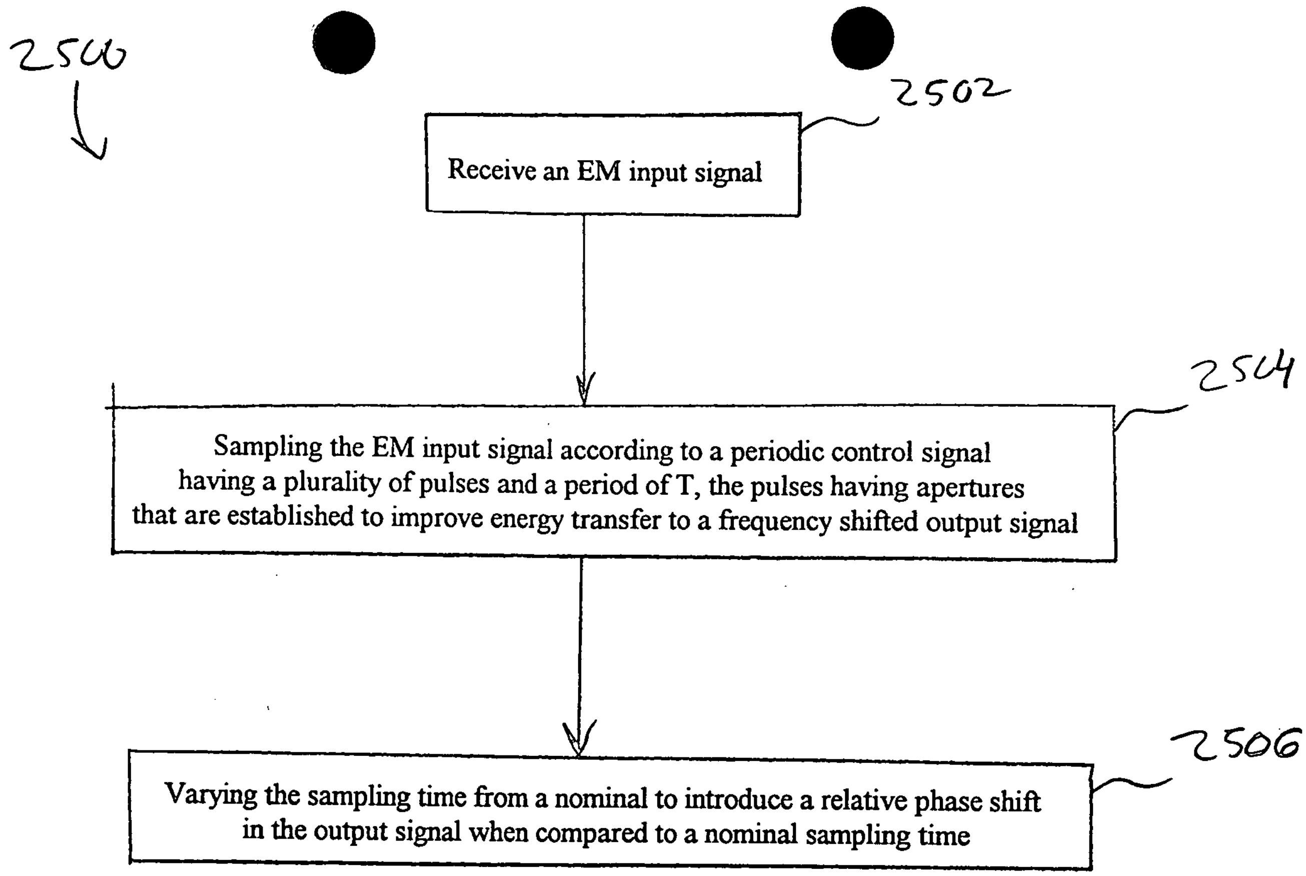

2500
2502
Receive an EM input signal
2504
Sampling the EM input signal according to a periodic control signal having a plurality of pulses and a period of T, the pulses having apertures that are established to improve energy transfer to a frequency shifted output signal
2506
Varying the sampling time from a nominal to introduce a relative phase shift in the output signal when compared to a nominal sampling time

FIG. 25D

FIG. 25E

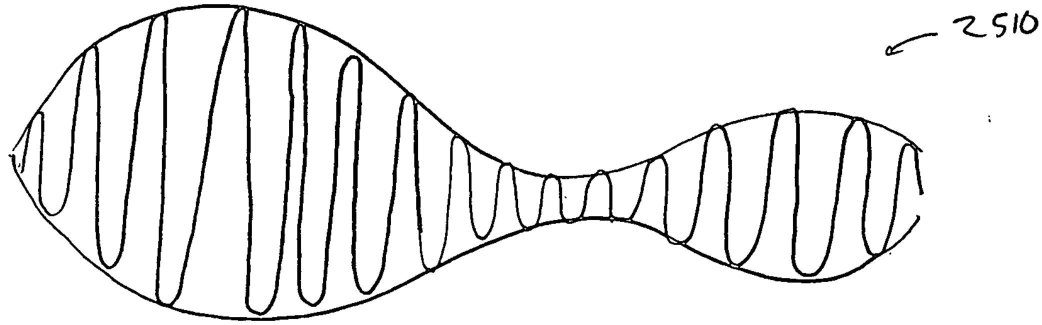


FIG. 25F

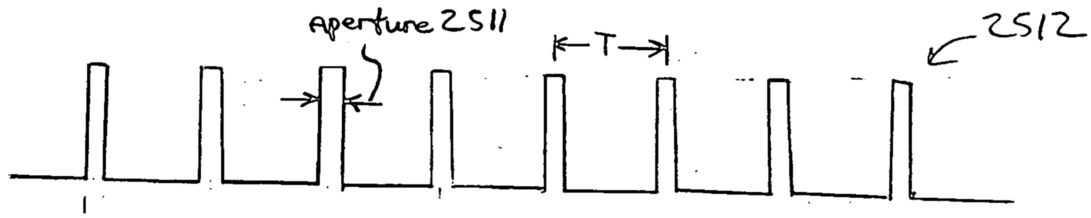
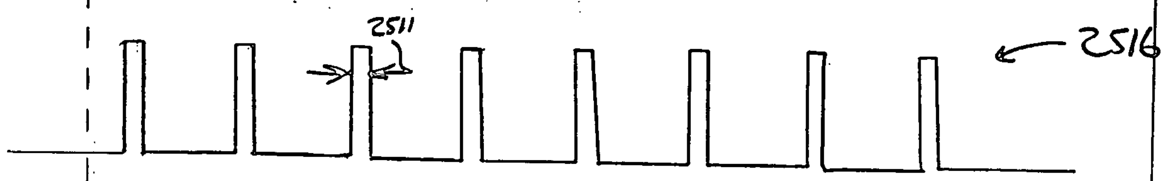


FIG. 25G

FIG. 25H



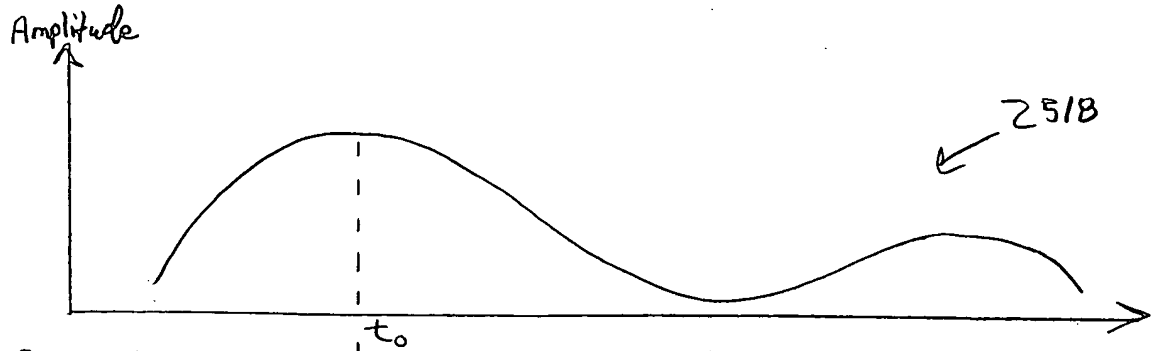


FIG. 25I

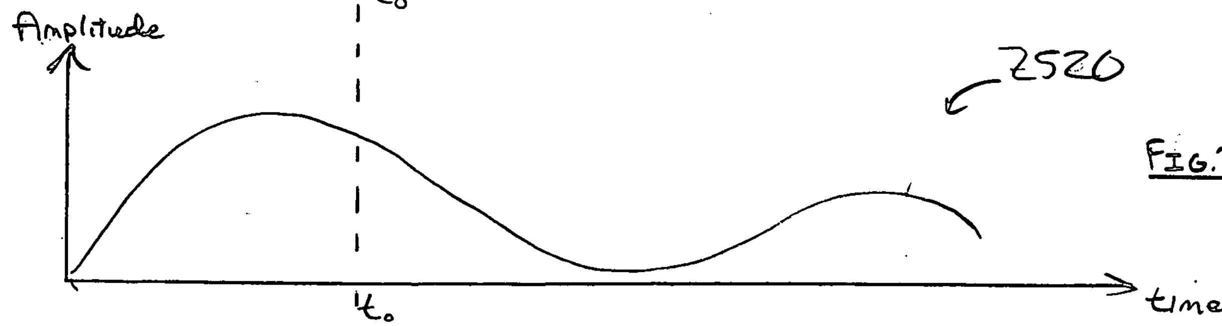


FIG. 25J

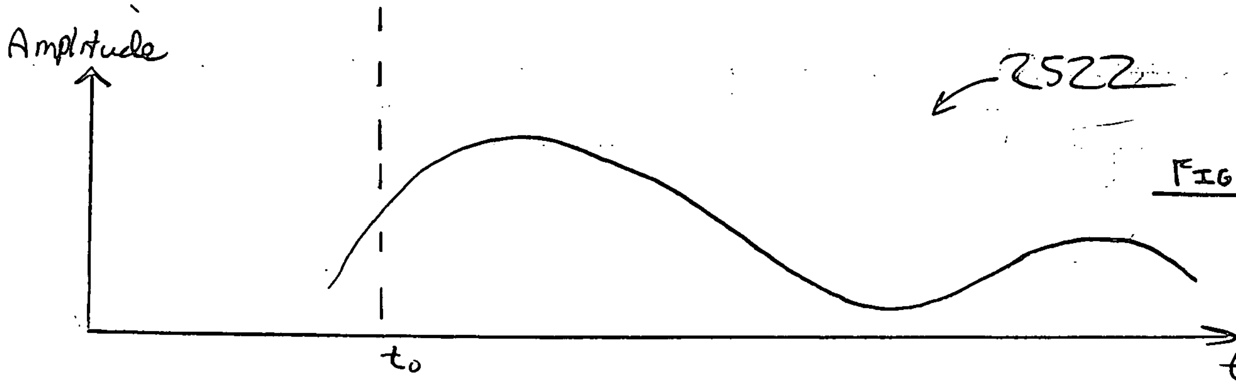


FIG. 25K

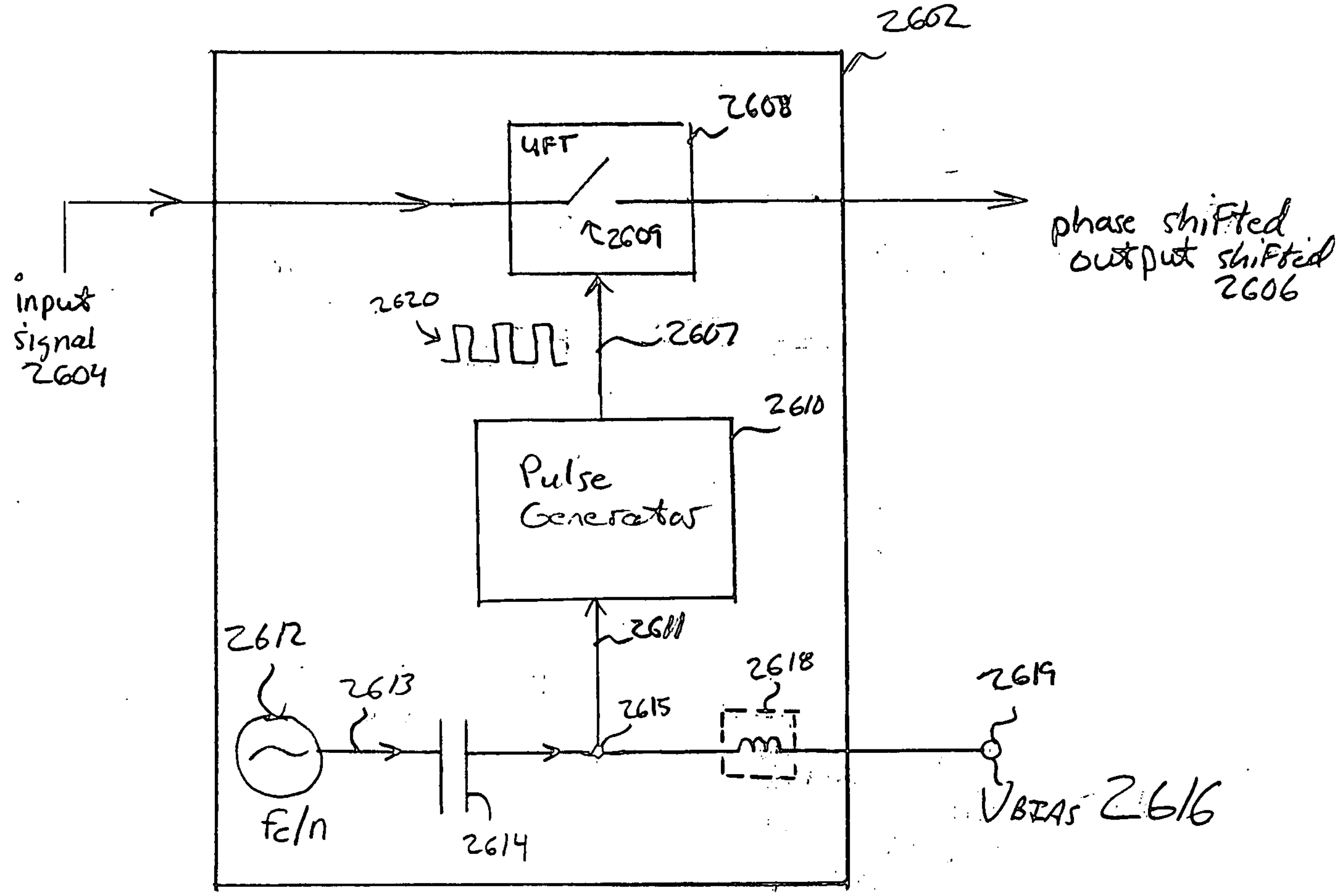

2602
2608
UFT
2609
input signal 2604
phase shifted output shifted 2606
2620
2607
2610
Pulse Generator
2611
2612
2613
2615
2618
2619
fc/n
2614
VBIAS 2616

FIG. 26A

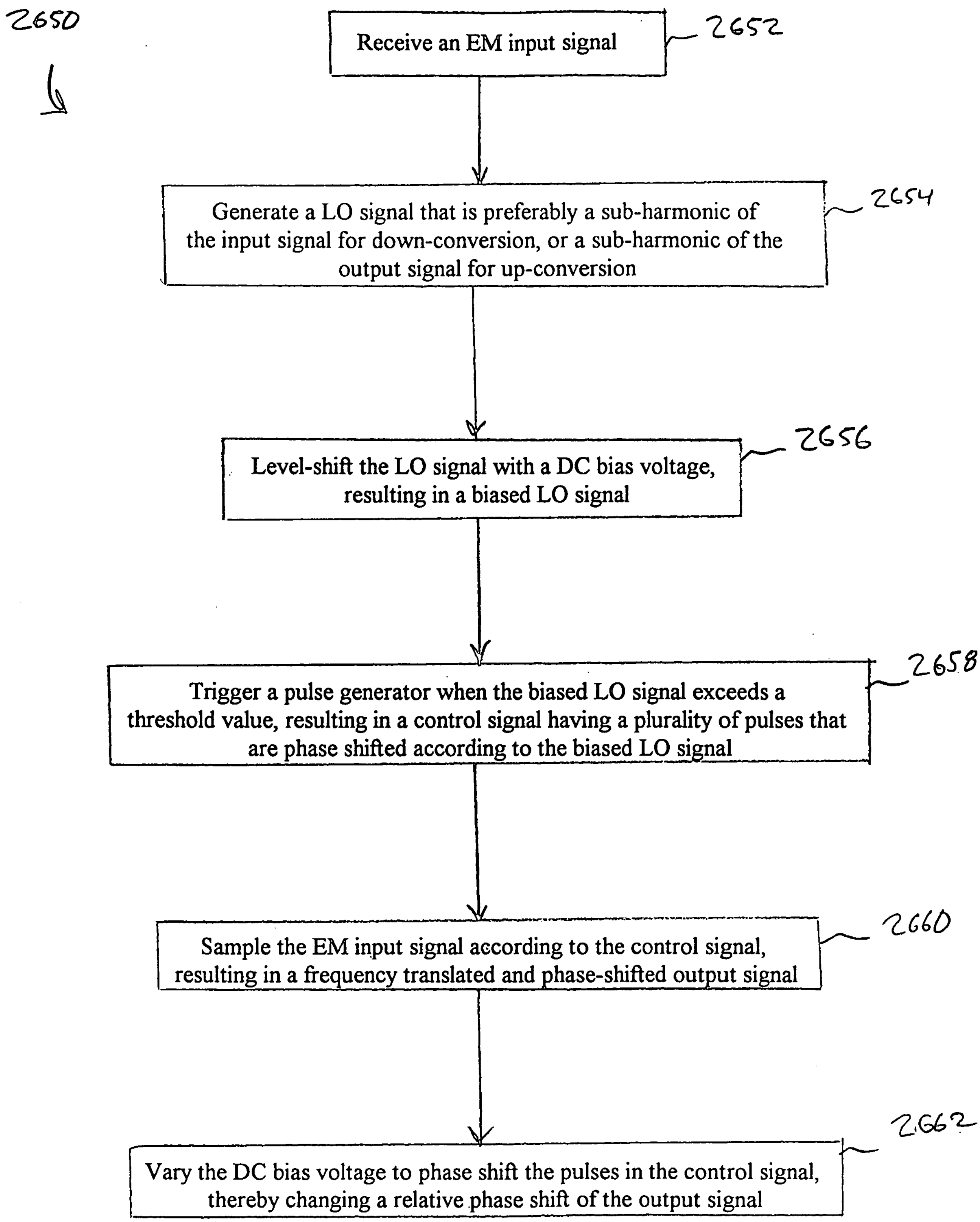

2650
Receive an EM input signal
2652
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion, or a sub-harmonic of the output signal for up-conversion
2654
Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal
2656
Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal
2658
Sample the EM input signal according to the control signal, resulting in a frequency translated and phase-shifted output signal
2660
Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
2662

FIG. 26B

FIG. 27A: $V_B = 0$ volts

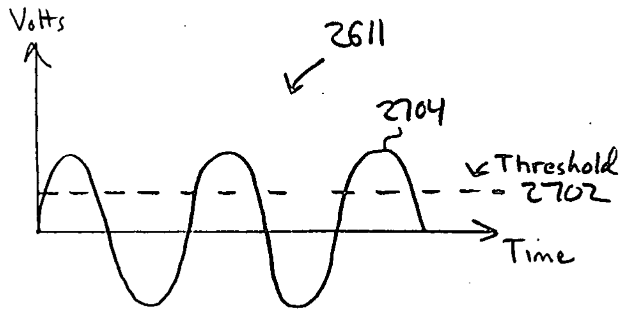


FIG. 27B: $V_B = +A$ volts

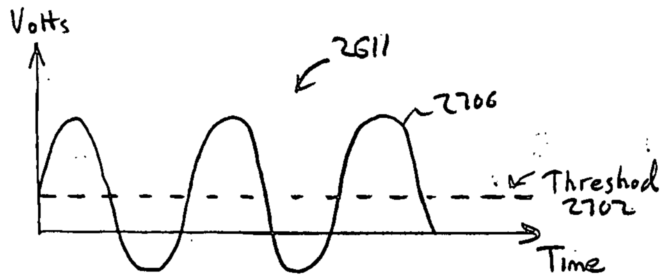


FIG. 27C: $V_B = -A$ volts

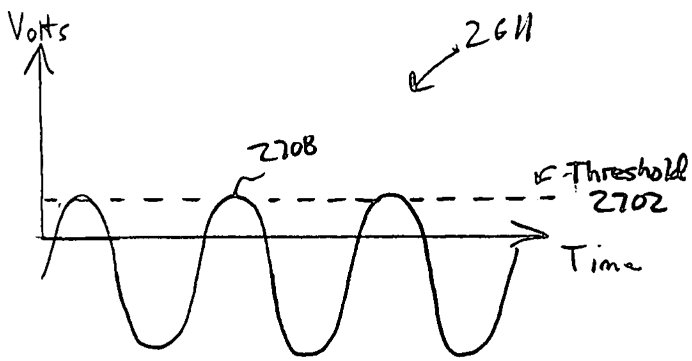
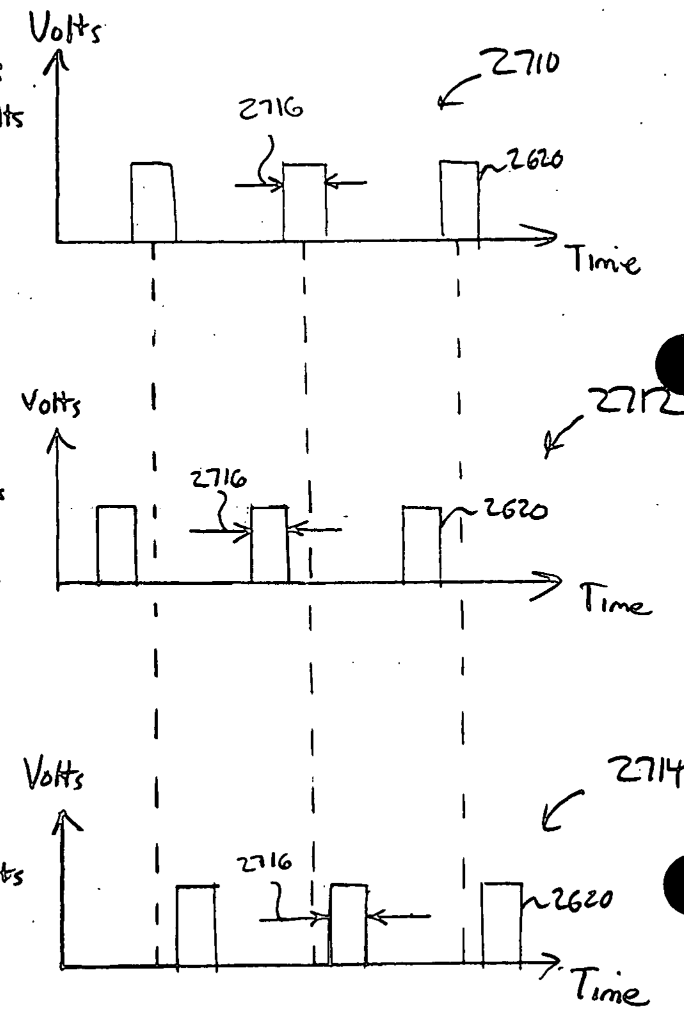


FIG. 27D: $V_B = 0$ volts

FIG. 27E: $V_B = +A$ volts

FIG. 27F: $V_B = -A$ volts



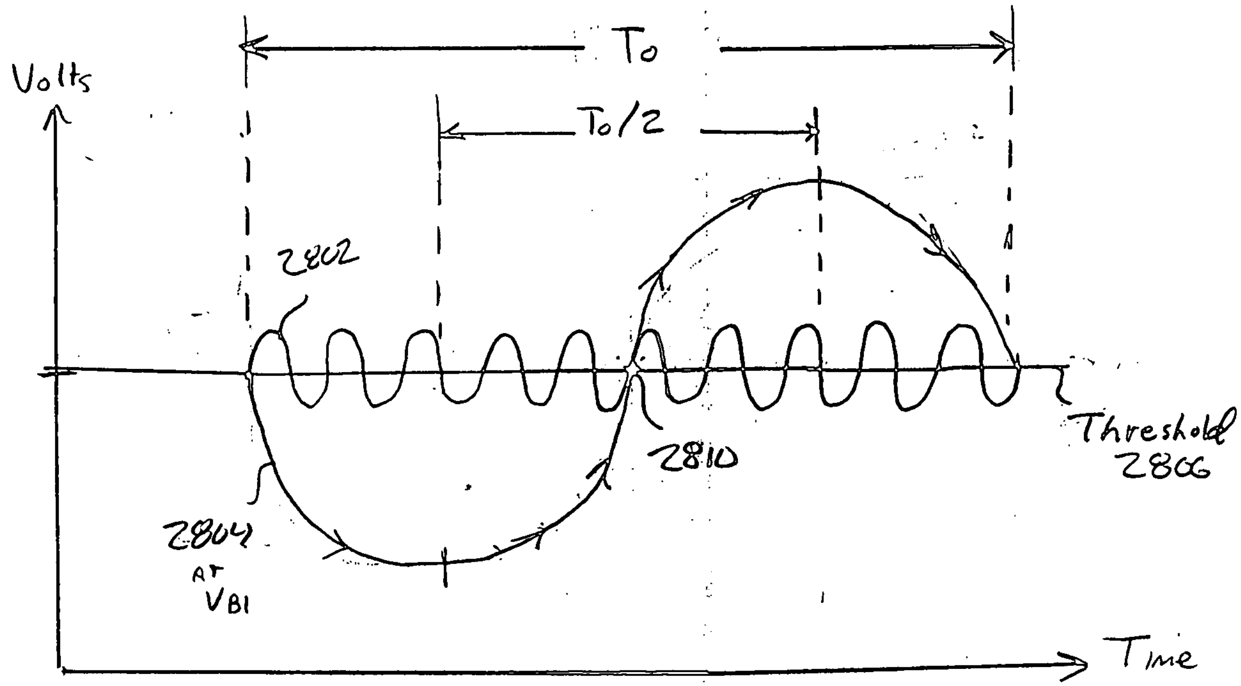


FIG. 28A

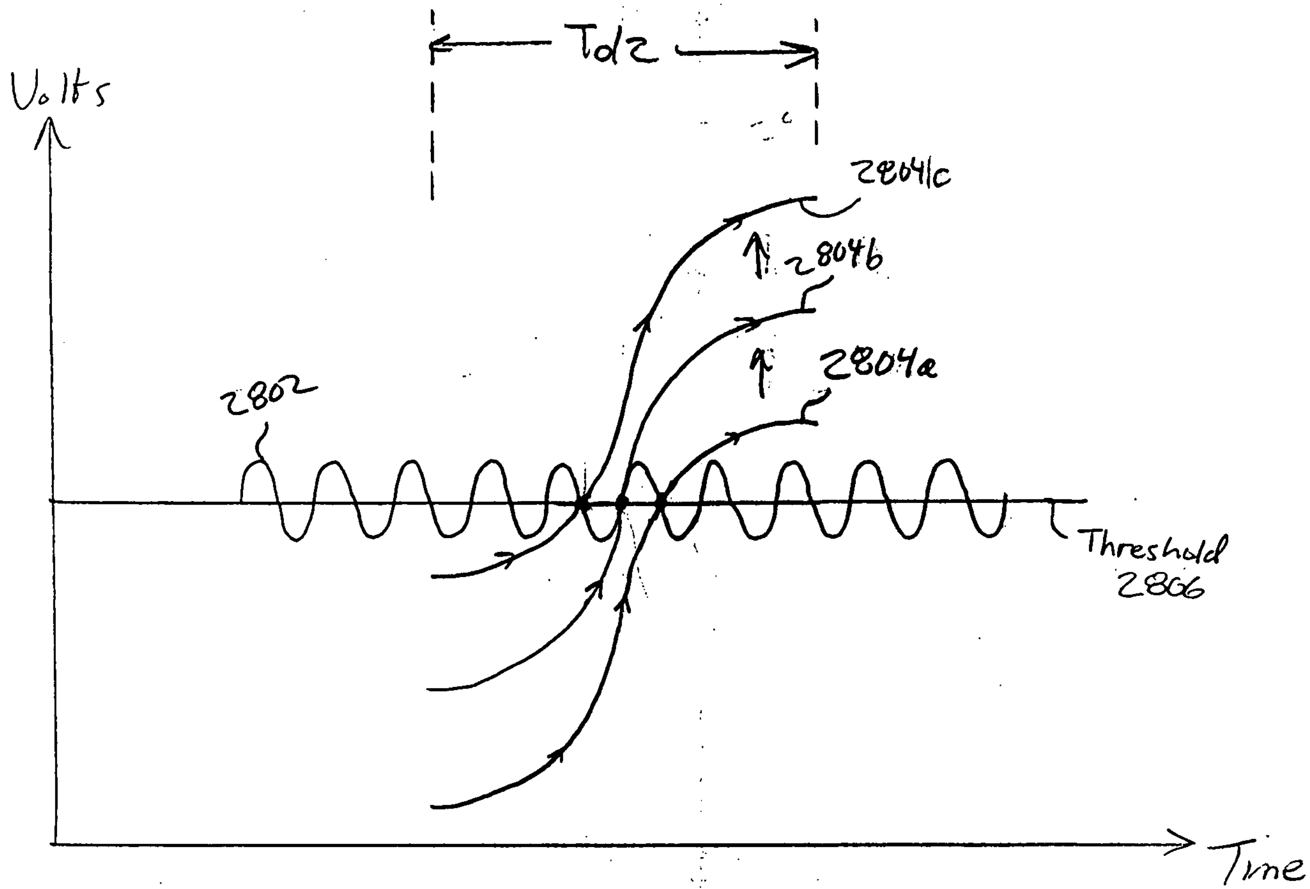


FIG. 28B

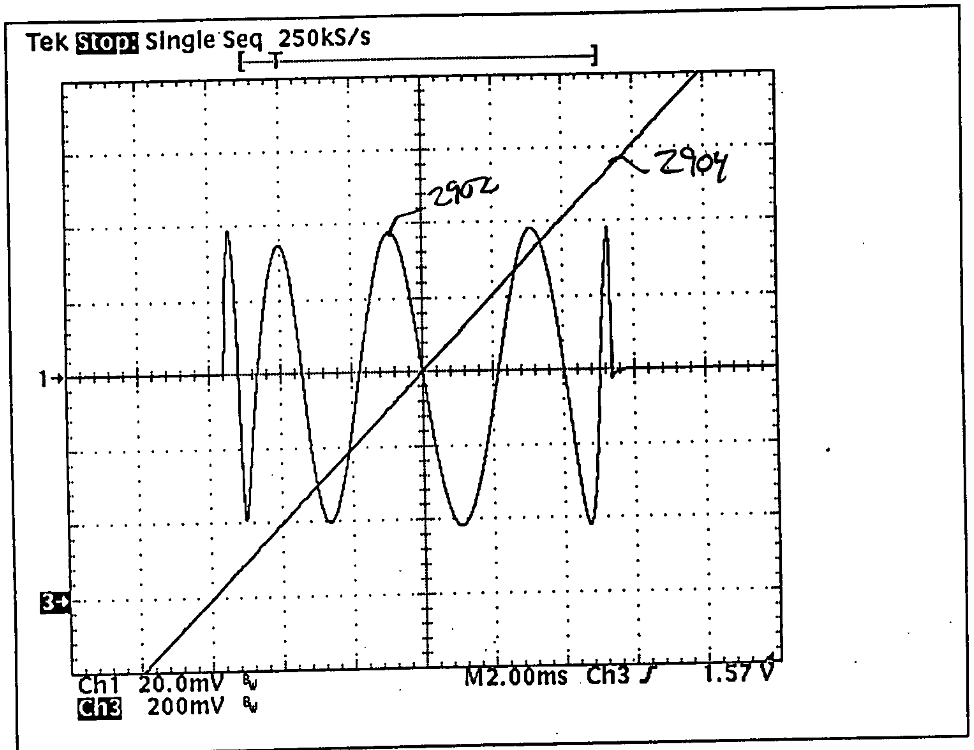
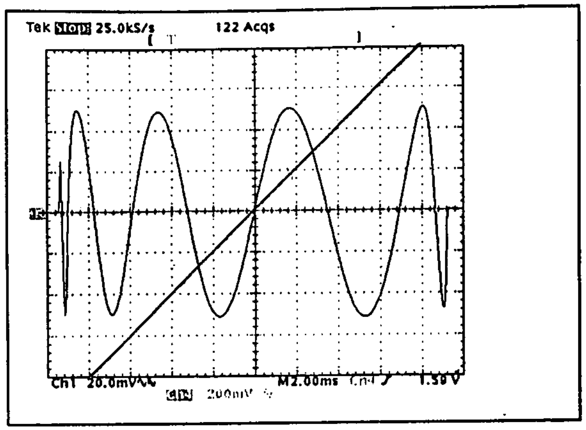

Tek Stop: Single Seq 250kS/s
2902
2904
1→
3→
Ch1 20.0mV
Ch3 200mV
M2.00ms Ch3 ∫ 1.57 V

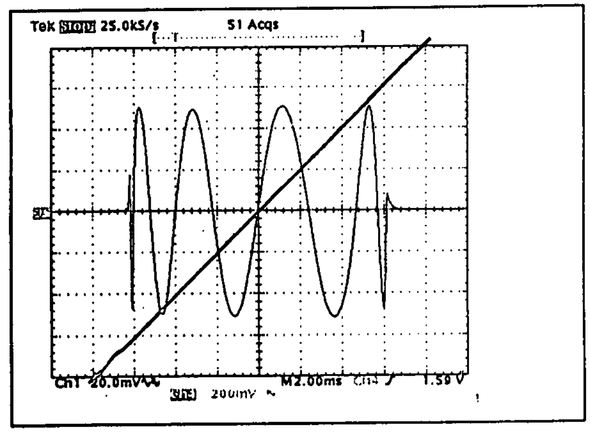
FIG. 29

FIG. 30A

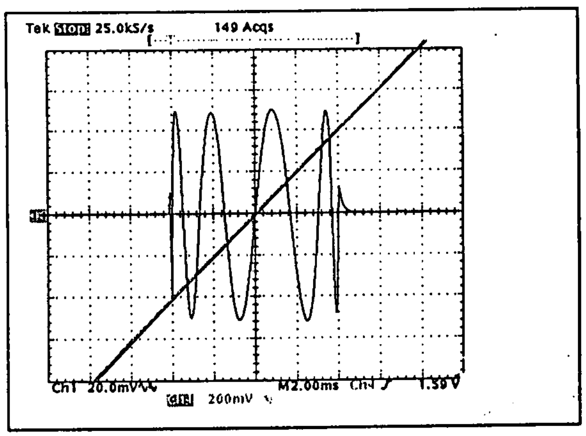


LO amplitude=1.415 $V_{p\text{-}p}$.

FIG. 30B

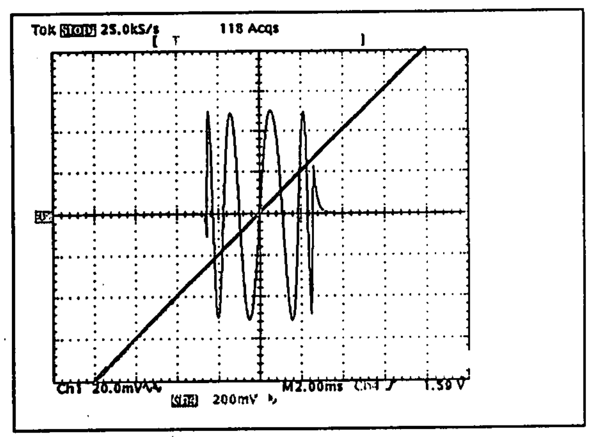


LO amplitude=1.002 $V_{p\text{-}p}$.



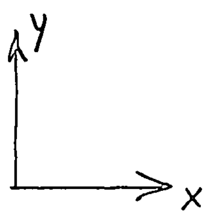
LO amplitude=0.710 $V_{p\text{-}p}$.

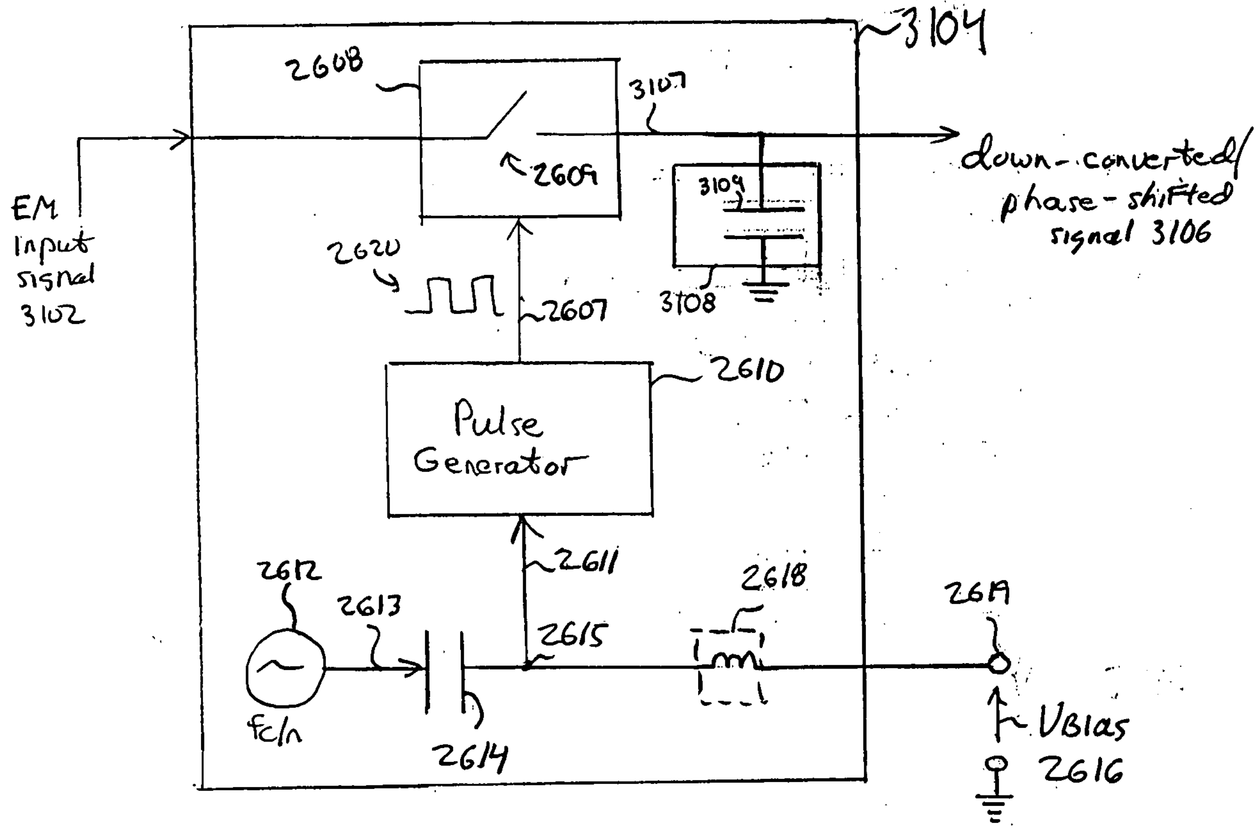
FIG. 30C



LO amplitude=0.502 $V_{p\text{-}p}$.

FIG. 30D





3104
2608
3107
2609
EM input signal 3102
down-converted/ phase-shifted signal 3106
3109
3108
2620
2607
2610
Pulse Generator
2611
2612
2613
2615
2618
2619
fc/n
2614
Vbias 2616

FIG. 31A

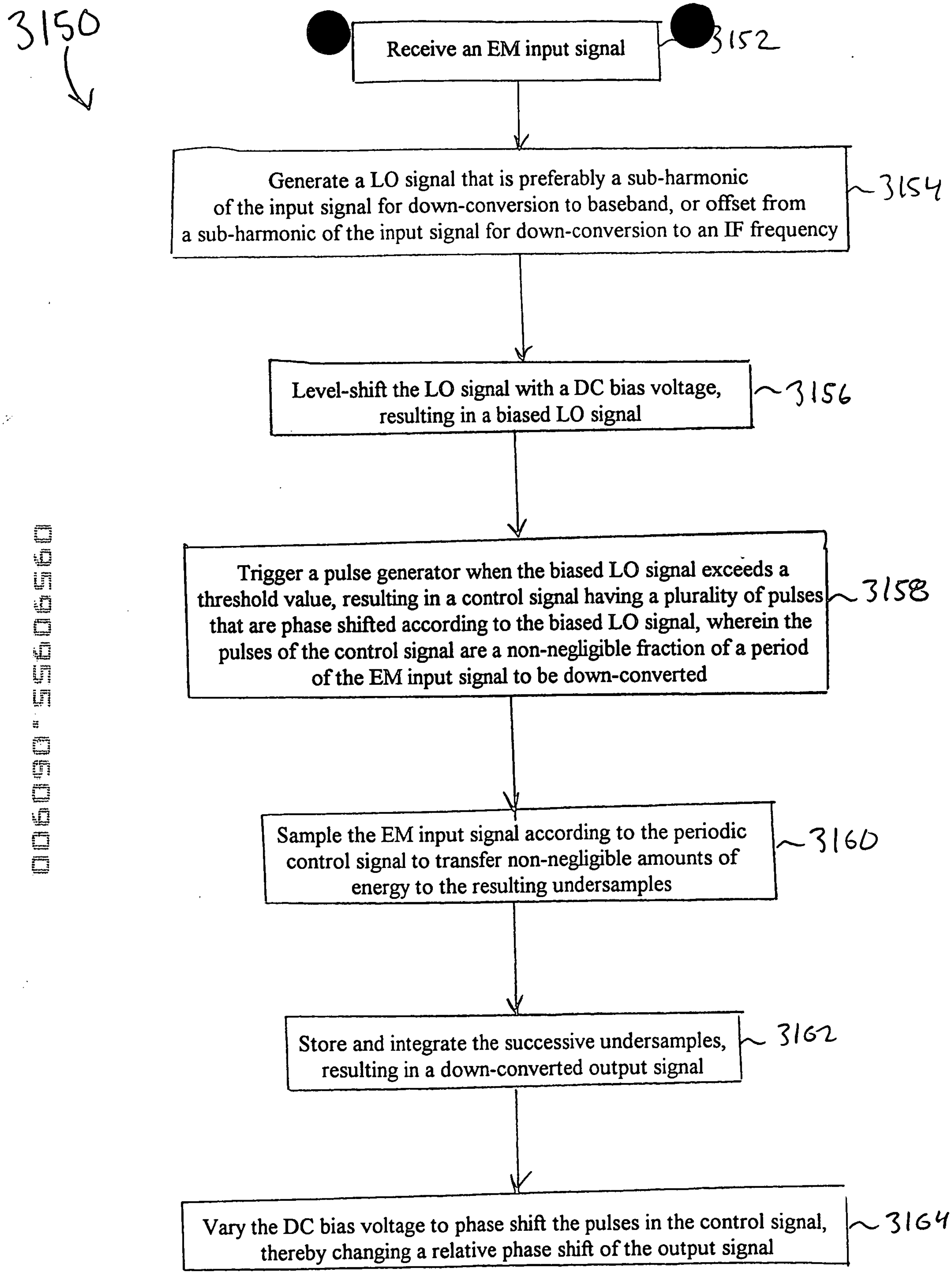

3150
Receive an EM input signal
3152
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion to baseband, or offset from a sub-harmonic of the input signal for down-conversion to an IF frequency
3154
Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal
3156
Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal, wherein the pulses of the control signal are a non-negligible fraction of a period of the EM input signal to be down-converted
3158
Sample the EM input signal according to the periodic control signal to transfer non-negligible amounts of energy to the resulting undersamples
3160
Store and integrate the successive undersamples, resulting in a down-converted output signal
3162
Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3164

FIG. 31B

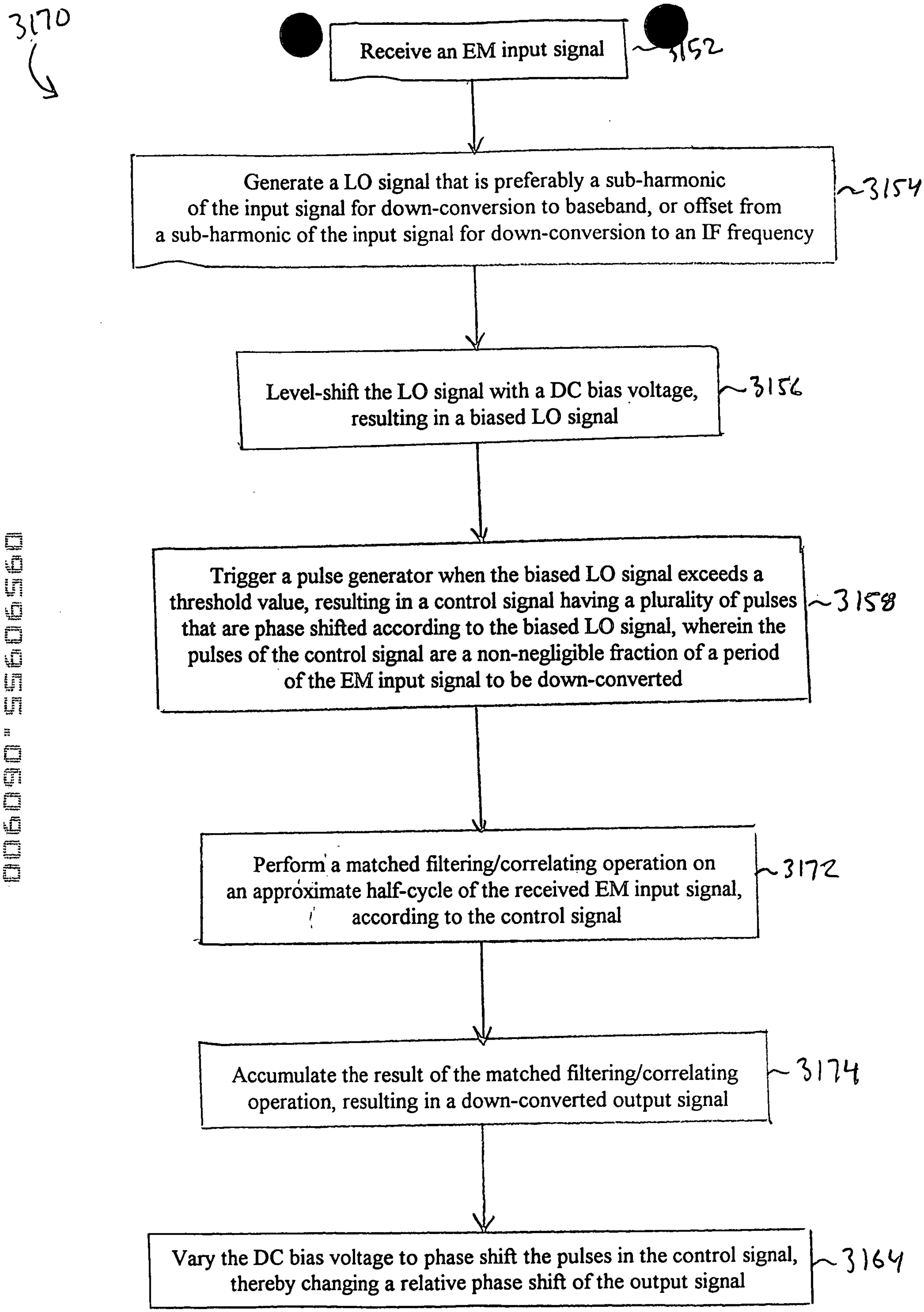

3170
Receive an EM input signal
3152
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion to baseband, or offset from a sub-harmonic of the input signal for down-conversion to an IF frequency
3154
Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal
3156
Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal, wherein the pulses of the control signal are a non-negligible fraction of a period of the EM input signal to be down-converted
3158
Perform a matched filtering/correlating operation on an approximate half-cycle of the received EM input signal, according to the control signal
3172
Accumulate the result of the matched filtering/correlating operation, resulting in a down-converted output signal
3174
Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3164

FIG 31C

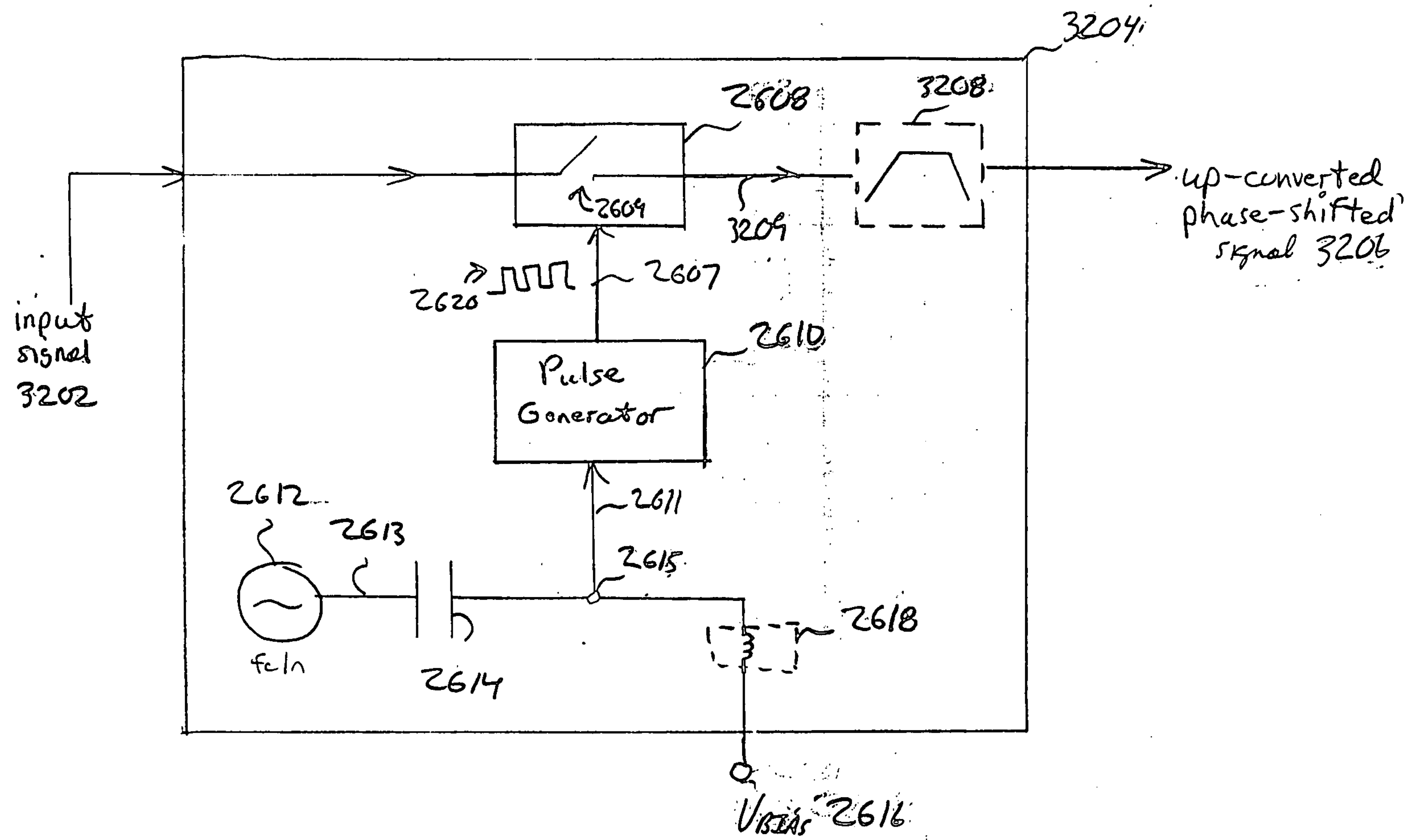

3204
3208
2608
2609
3209
up-converted
phase-shifted
signal 3206
input
signal
3202
2620
2607
2610
Pulse
Generator
2611
2612
2613
2615
2618
fcln
2614
V_{BIAS} 2616

FIG. 32A

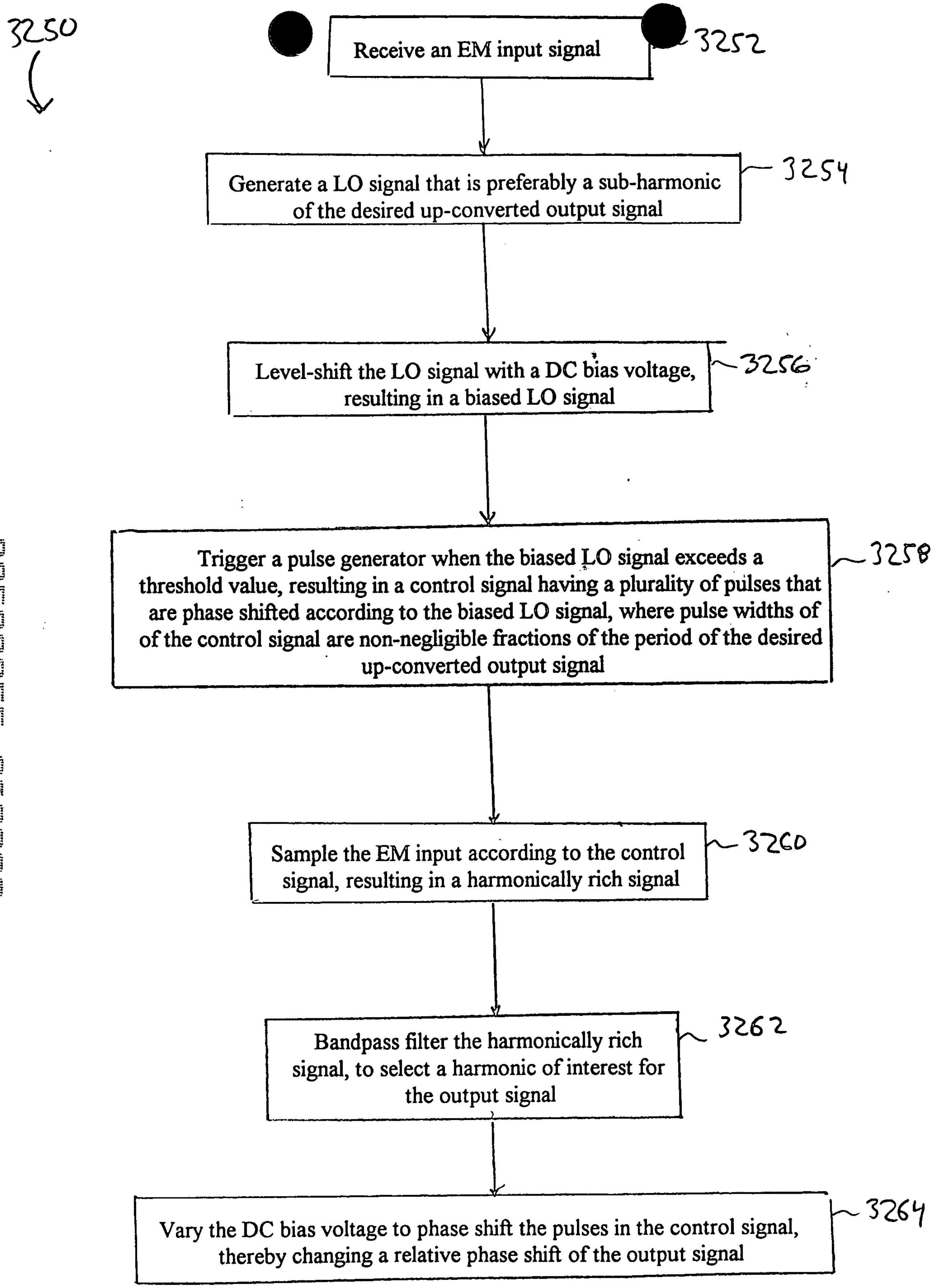

3250
Receive an EM input signal
3252
Generate a LO signal that is preferably a sub-harmonic of the desired up-converted output signal
3254
Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal
3256
Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal, where pulse widths of of the control signal are non-negligible fractions of the period of the desired up-converted output signal
3258
Sample the EM input according to the control signal, resulting in a harmonically rich signal
3260
Bandpass filter the harmonically rich signal, to select a harmonic of interest for the output signal
3262
Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3264

FIG. 32B

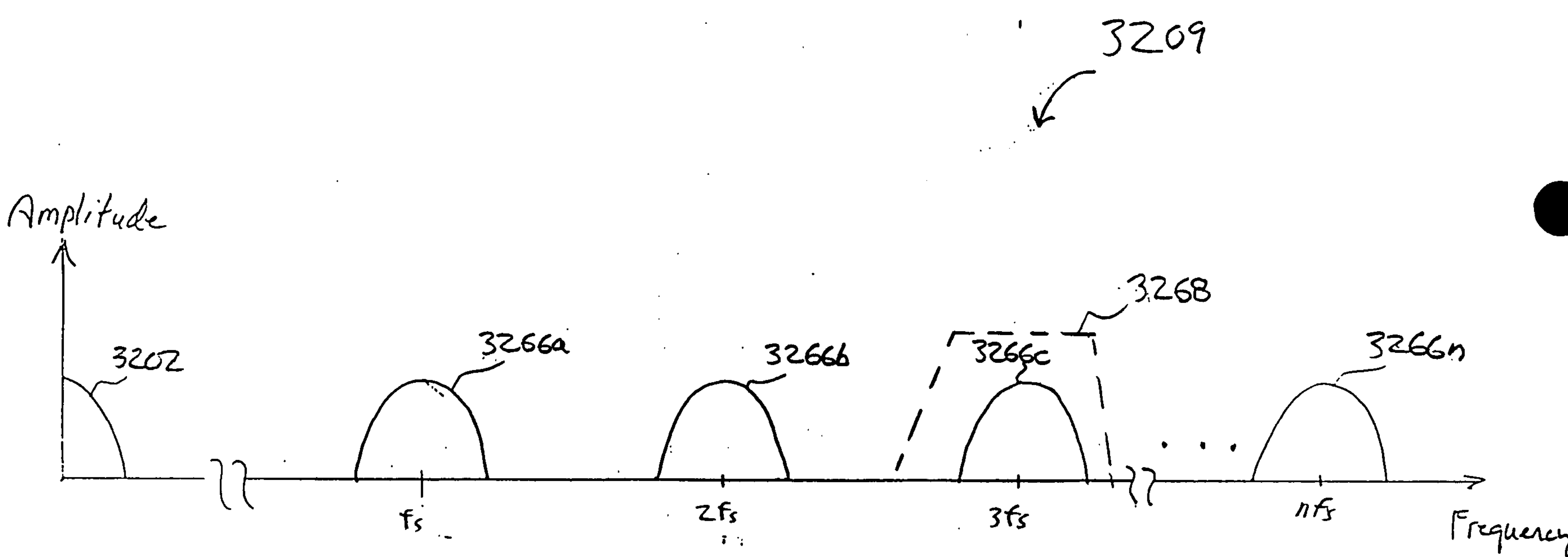

3209
Amplitude
3202
3266a
3266b
3268
3266c
3266n
fs
2fs
3fs
nfs
Frequency

FIG. 32C

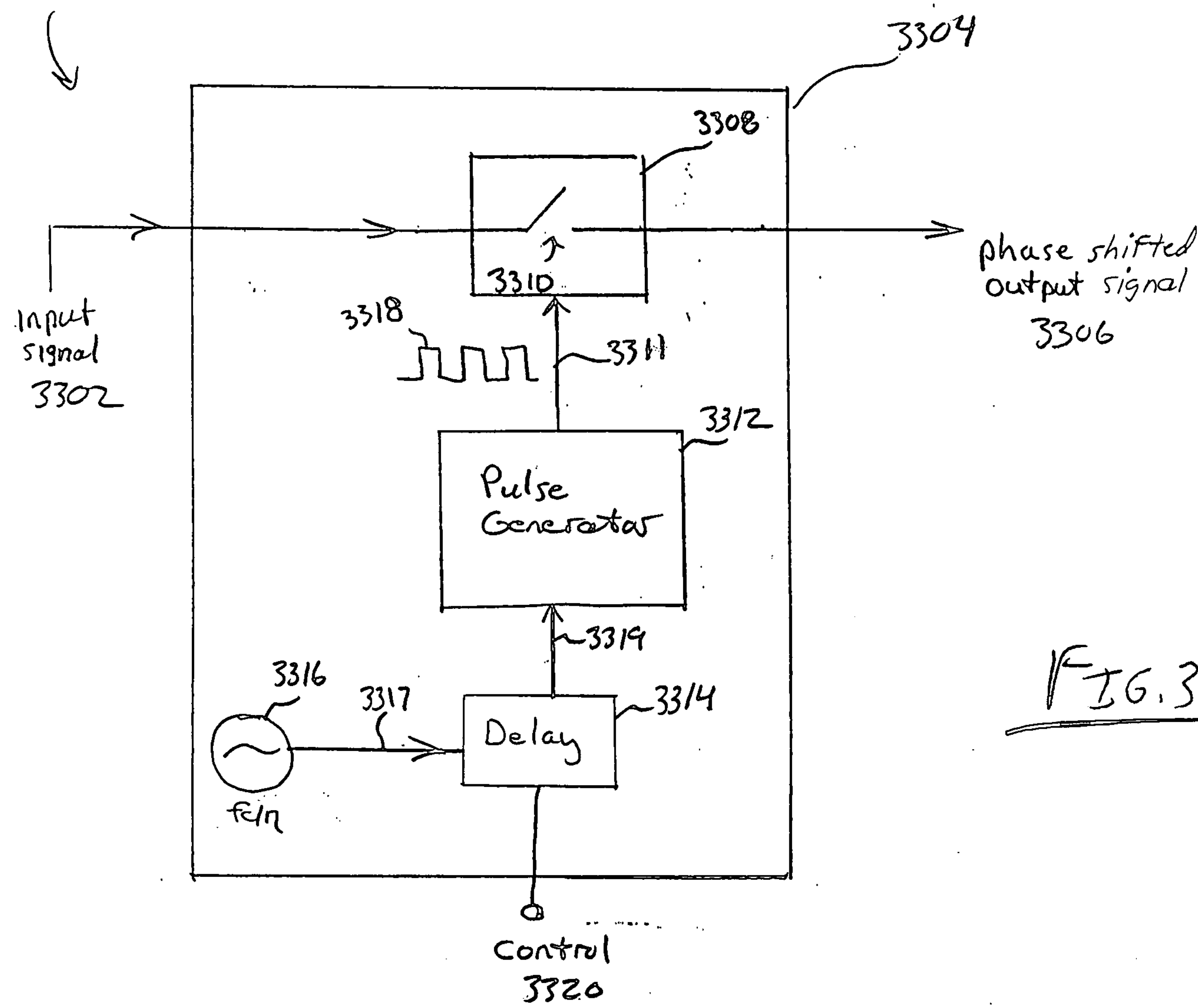

3304
3308
3310
phase shifted output signal 3306
input signal 3302
3318
3311
3312
Pulse Generator
3319
3316
3317
3314
Delay
fc/n
Control 3320

FIG. 33A

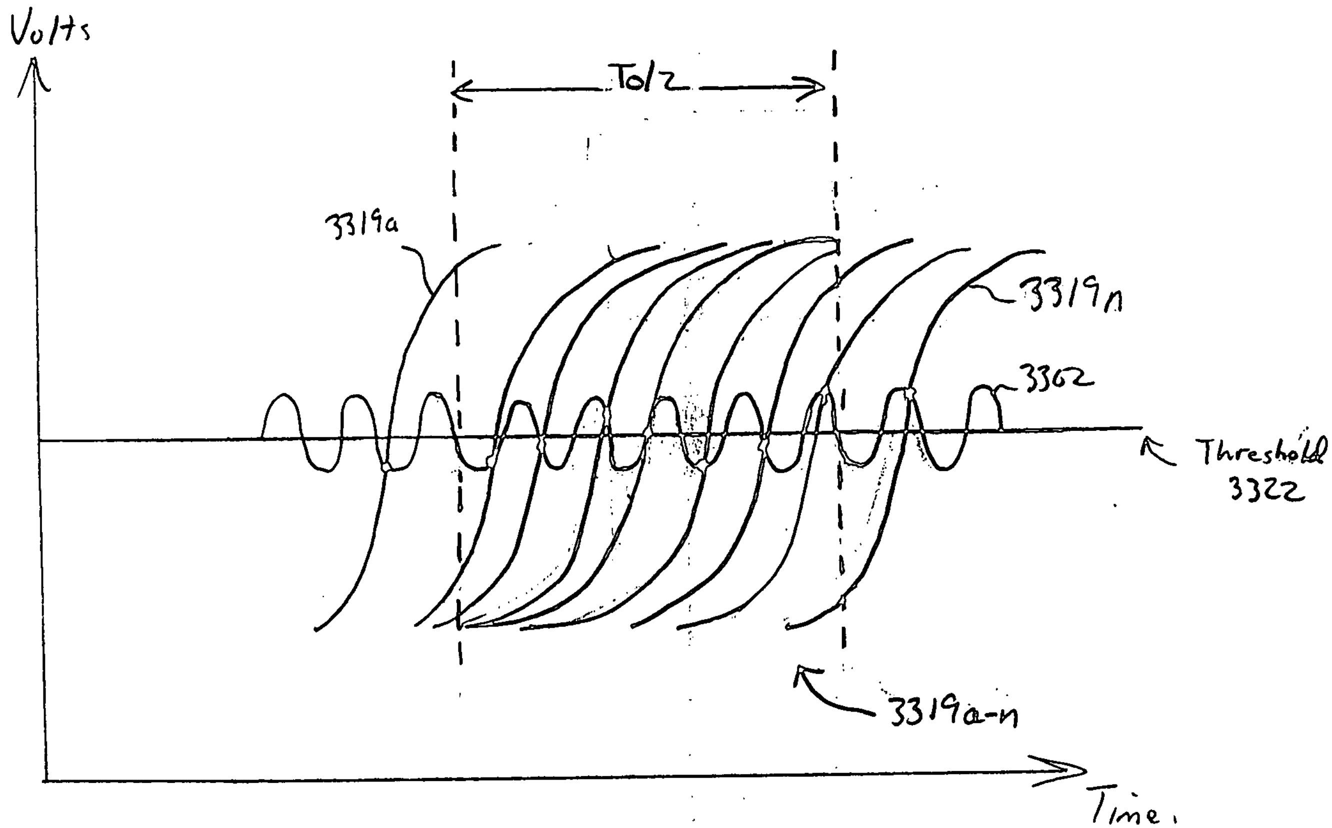


FIG. 33B

3350

Receive an EM input signal 3352

Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion, or a sub-harmonic of the output signal for up-conversion 3354

Delay the LO signal according to a control signal, resulting in a delayed LO signal 3356

Trigger a pulse generator when the delayed LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal 3358

Sample the EM input signal according to the control signal, resulting in a frequency translated and phase-shifted output signal 3360

Vary the delay of the LO signal to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal 3362

FIG. 33C

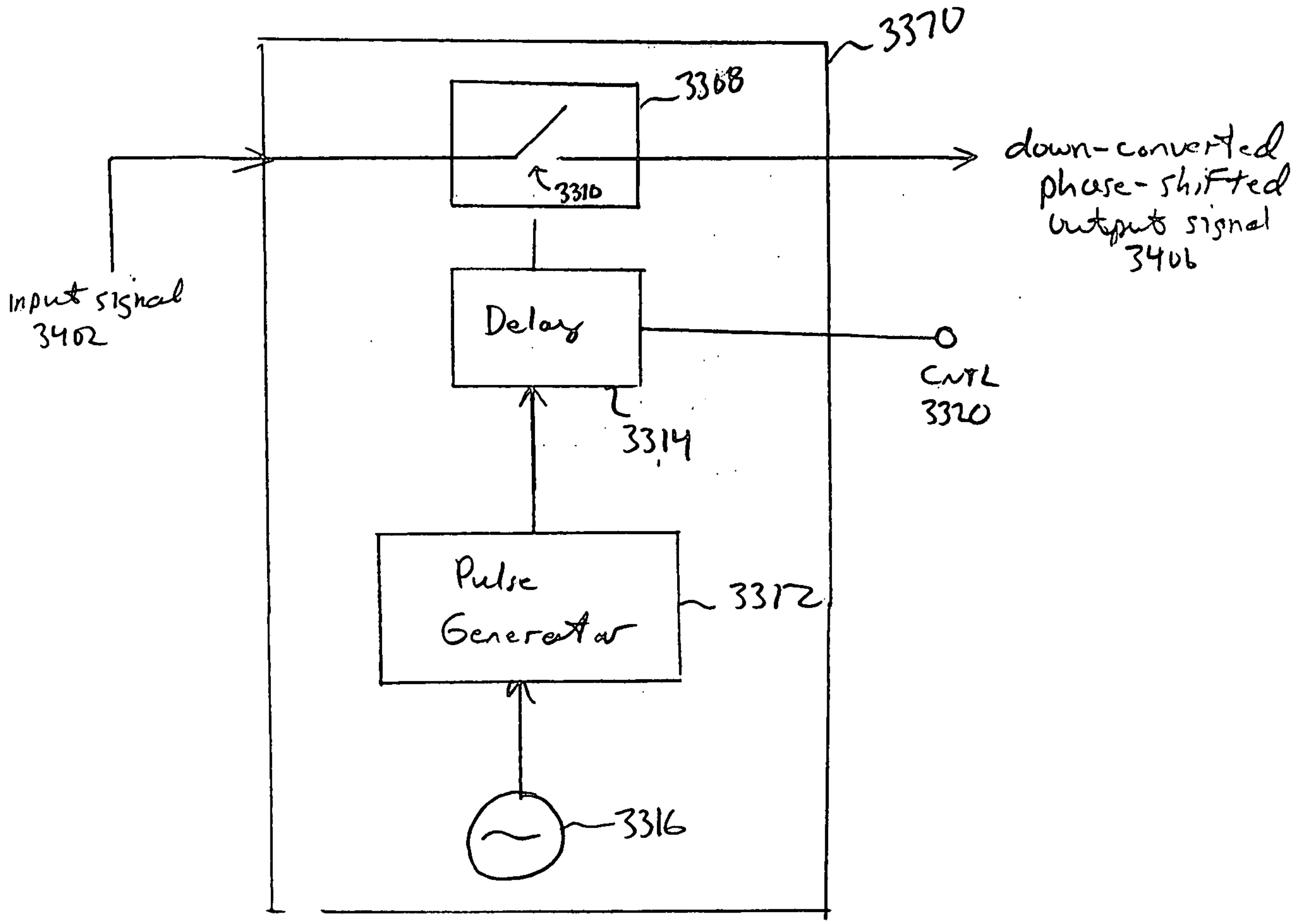

3370
3308
3310
input signal
3402
down-converted
phase-shifted
output signal
3406
Delay
3314
CNTL
3320
Pulse
Generator
3312
3316

FIG. 33D

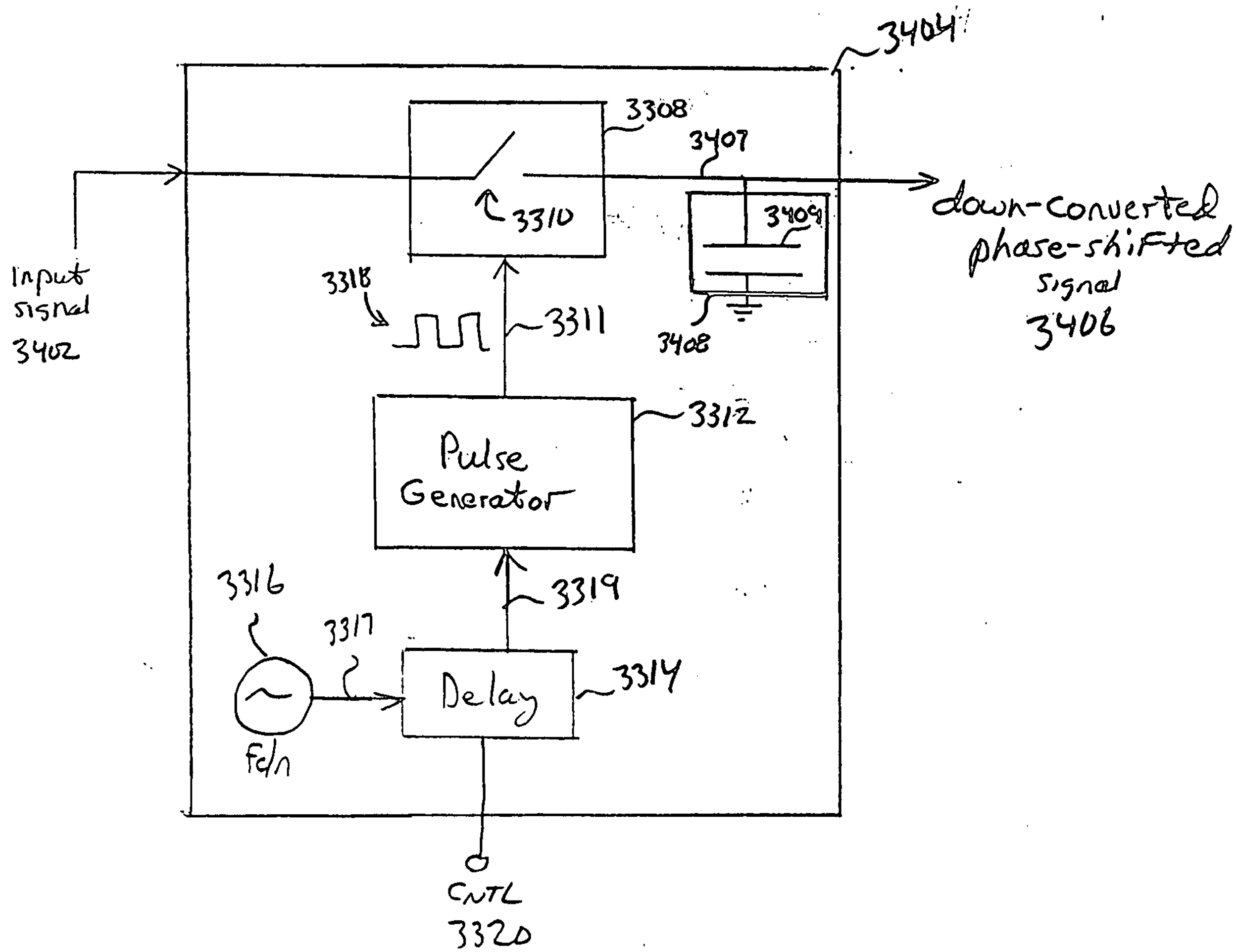
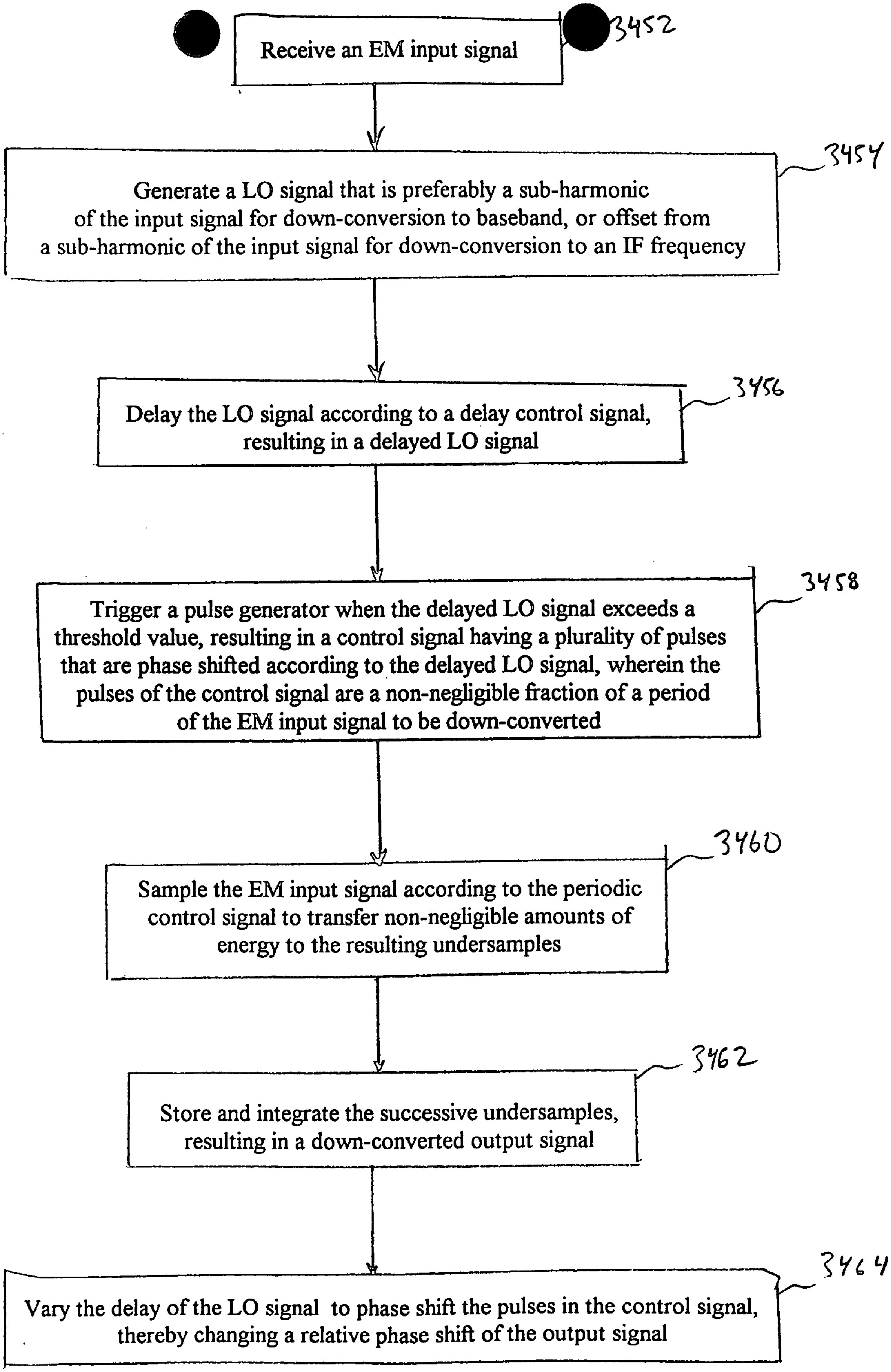

3404
3308
3407
3310
3409
Input signal 3402
3318
3311
3408
down-converted phase-shifted signal 3406
Pulse Generator
3312
3316
3319
3317
Delay
3314
Fc/n
CNTL 3320

FIG. 34A



Receive an EM input signal
3452
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion to baseband, or offset from a sub-harmonic of the input signal for down-conversion to an IF frequency
3454
Delay the LO signal according to a delay control signal, resulting in a delayed LO signal
3456
Trigger a pulse generator when the delayed LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the delayed LO signal, wherein the pulses of the control signal are a non-negligible fraction of a period of the EM input signal to be down-converted
3458
Sample the EM input signal according to the periodic control signal to transfer non-negligible amounts of energy to the resulting undersamples
3460
Store and integrate the successive undersamples, resulting in a down-converted output signal
3462
Vary the delay of the LO signal to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3464

FIG. 34B

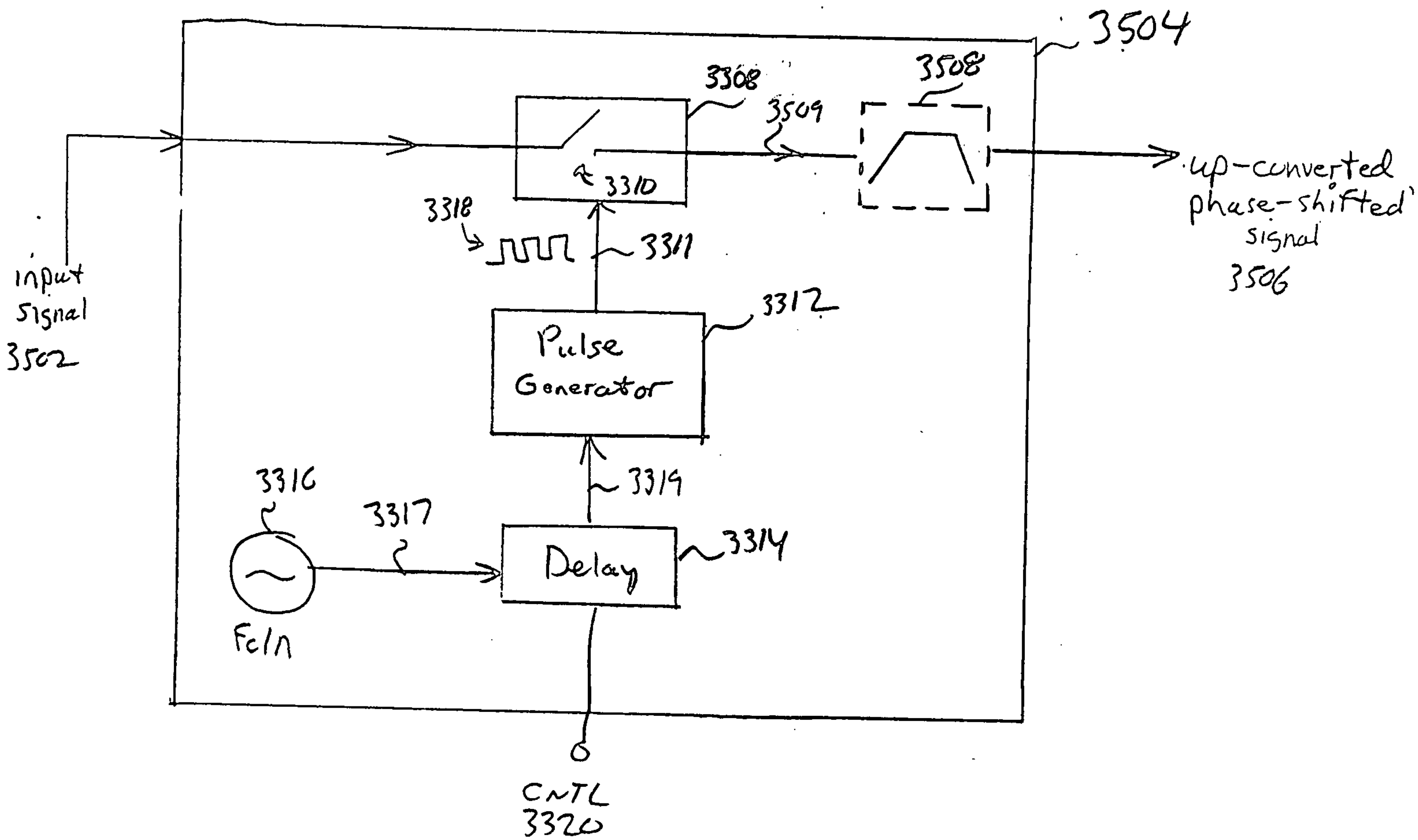

3504
3308
3508
3509
3310
up-converted
phase-shifted
signal
3506
3318
3311
input
signal
3502
3312
Pulse
Generator
3319
3316
3317
Delay
3314
Fc/n
CNTL
3320

FIG. 35A

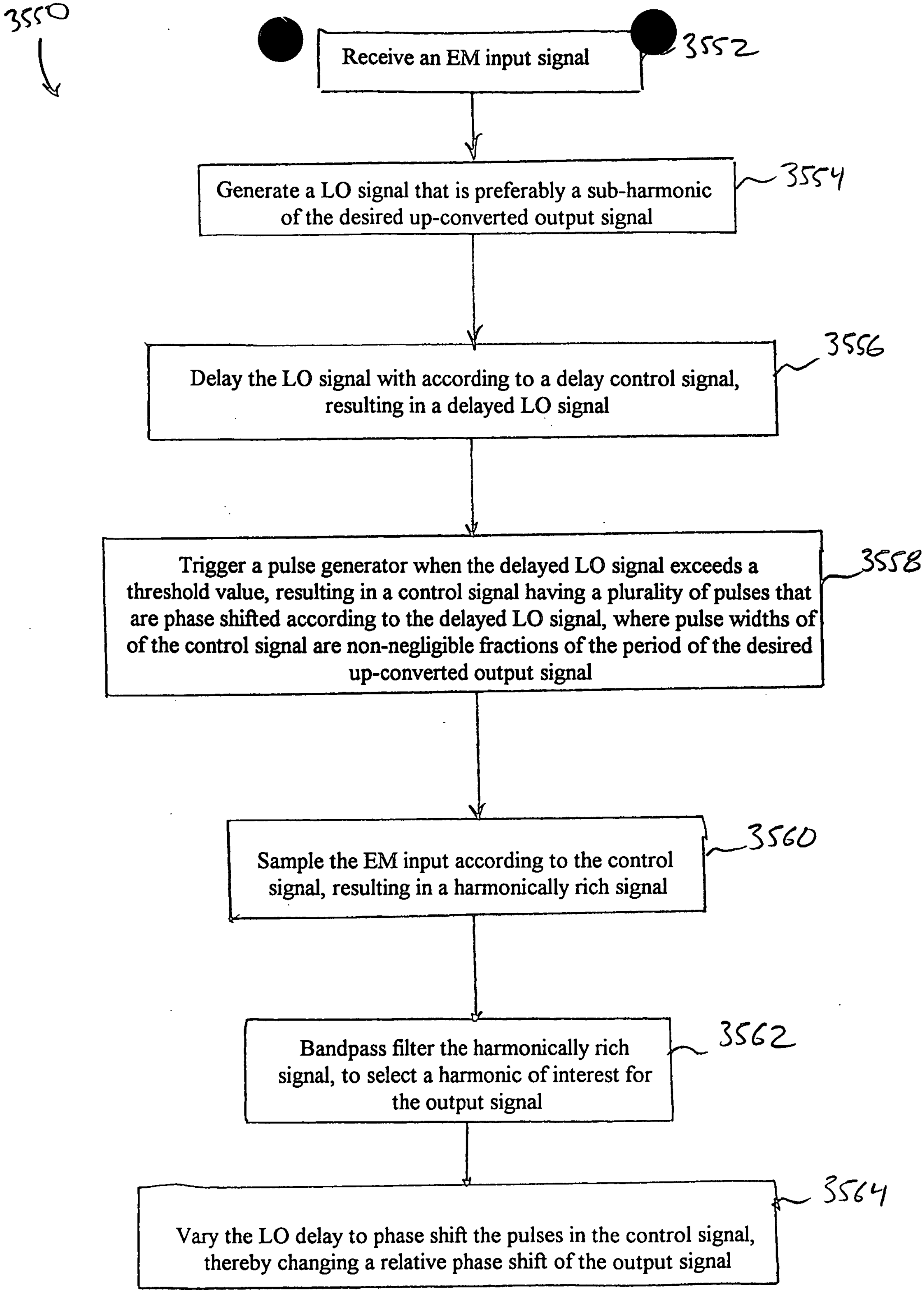

3550
Receive an EM input signal
3552
Generate a LO signal that is preferably a sub-harmonic of the desired up-converted output signal
3554
Delay the LO signal with according to a delay control signal, resulting in a delayed LO signal
3556
Trigger a pulse generator when the delayed LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the delayed LO signal, where pulse widths of of the control signal are non-negligible fractions of the period of the desired up-converted output signal
3558
Sample the EM input according to the control signal, resulting in a harmonically rich signal
3560
Bandpass filter the harmonically rich signal, to select a harmonic of interest for the output signal
3562
Vary the LO delay to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3564

FIG. 35B

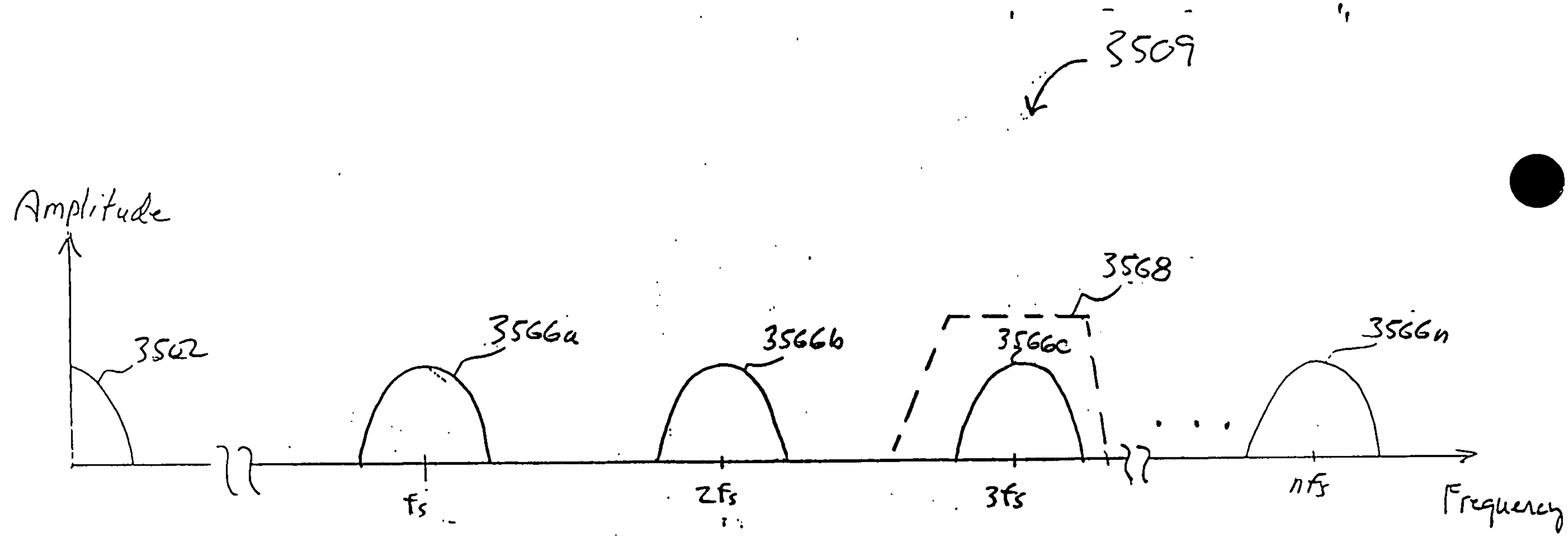

3509
Amplitude
3562
3566a
3566b
3568
3566c
3566n
fs
2fs
3fs
nfs
Frequency

FIG. 35C

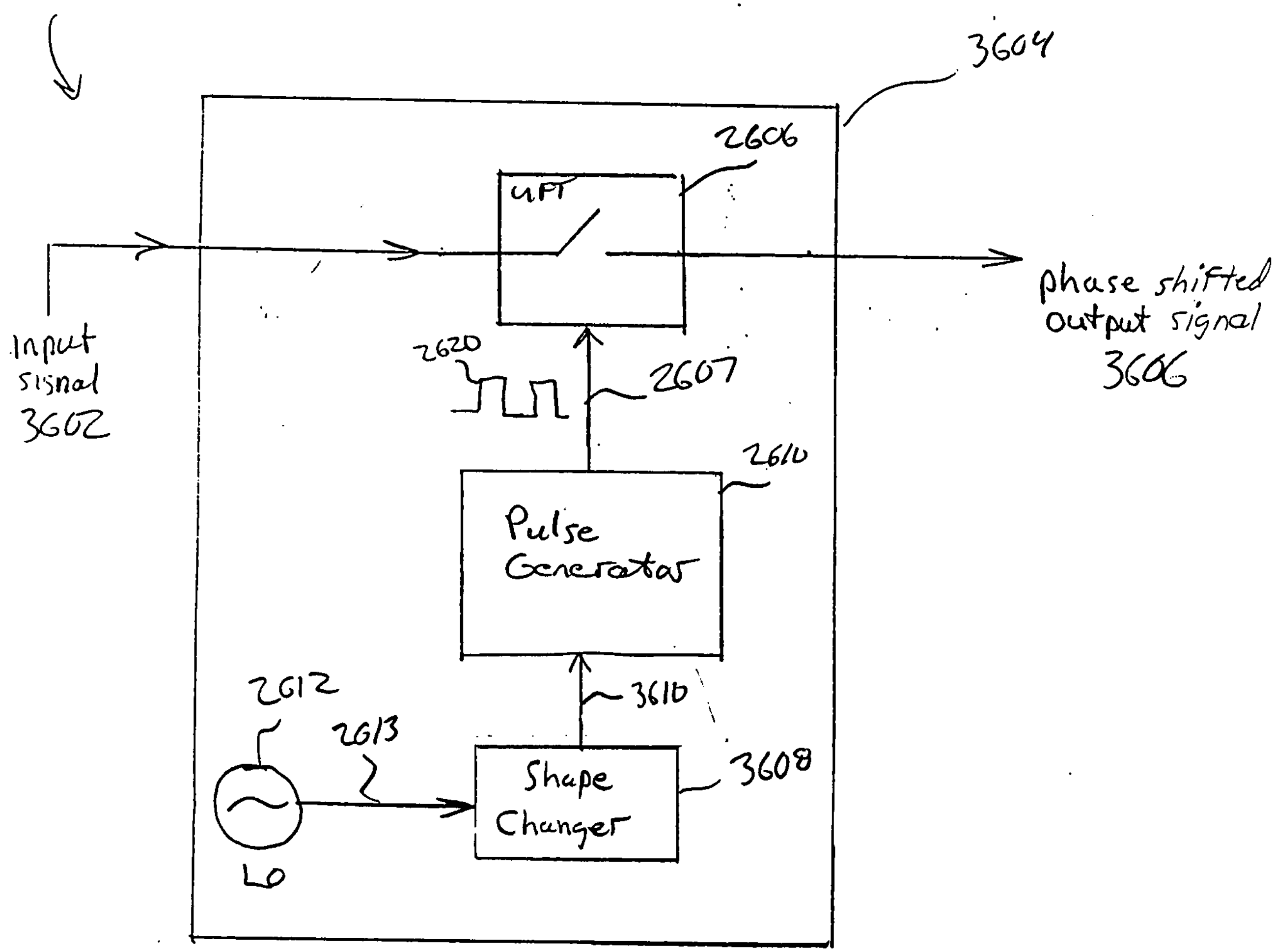

3604
2606
UFT
Input
signal
3602
phase shifted
output signal
3606
2620
2607
2610
Pulse
Generator
2612
2613
3610
Shape
Changer
3608
LO

FIG. 36

00609055 "060900

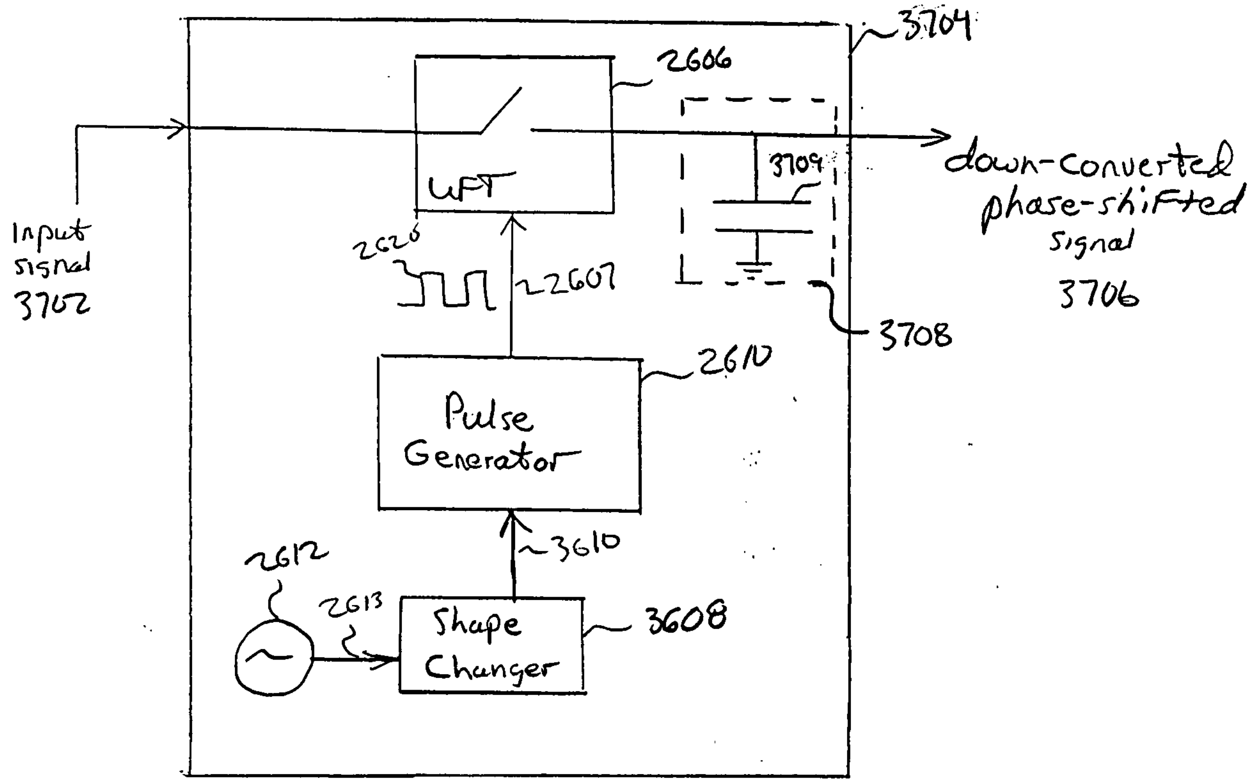


FIG. 37

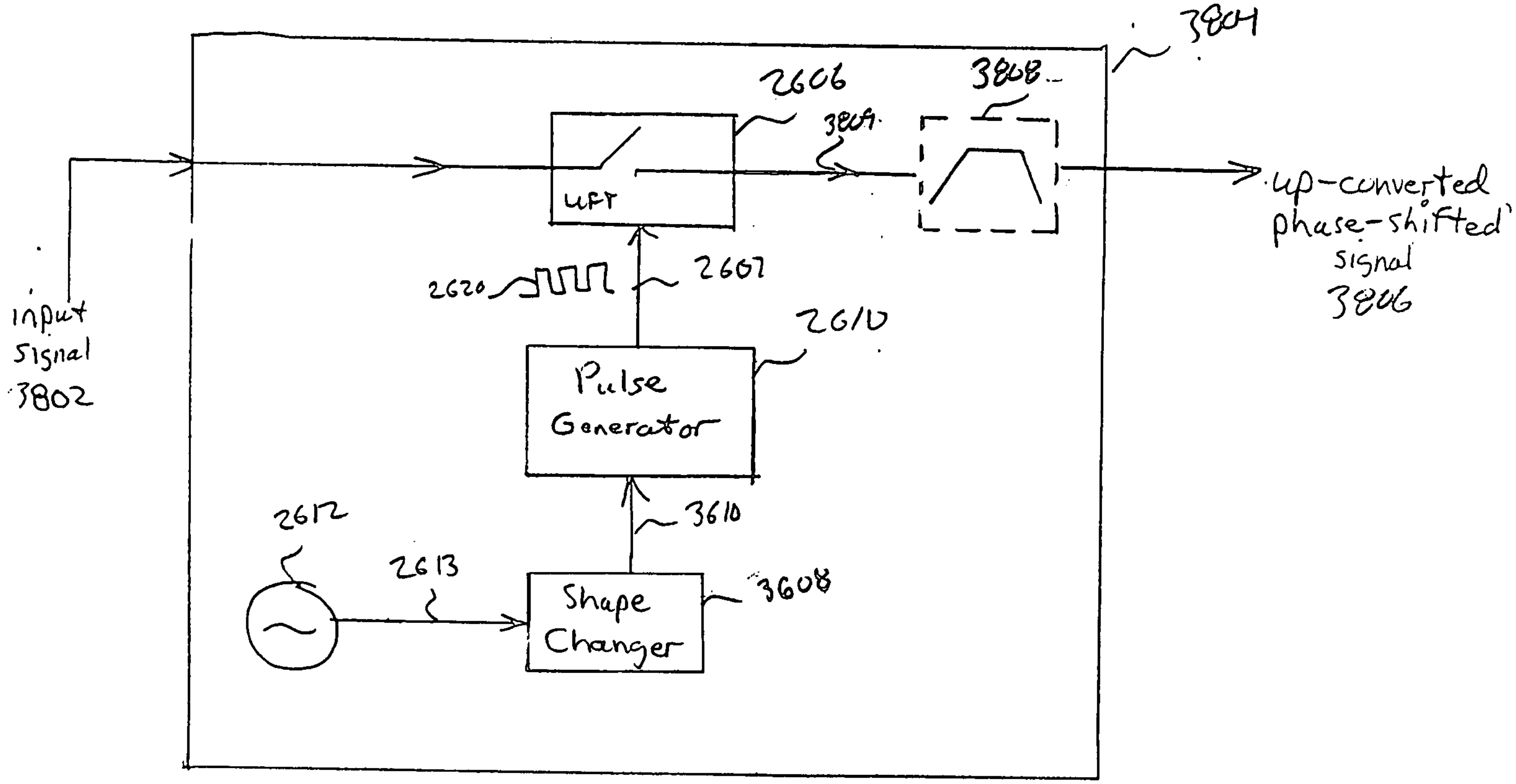

3804
2606
3808
3804
UFT
2620
2607
2610
Pulse Generator
2612
3610
2613
Shape Changer
3608
input signal 3802
up-converted phase-shifted signal 3806

FIG. 38

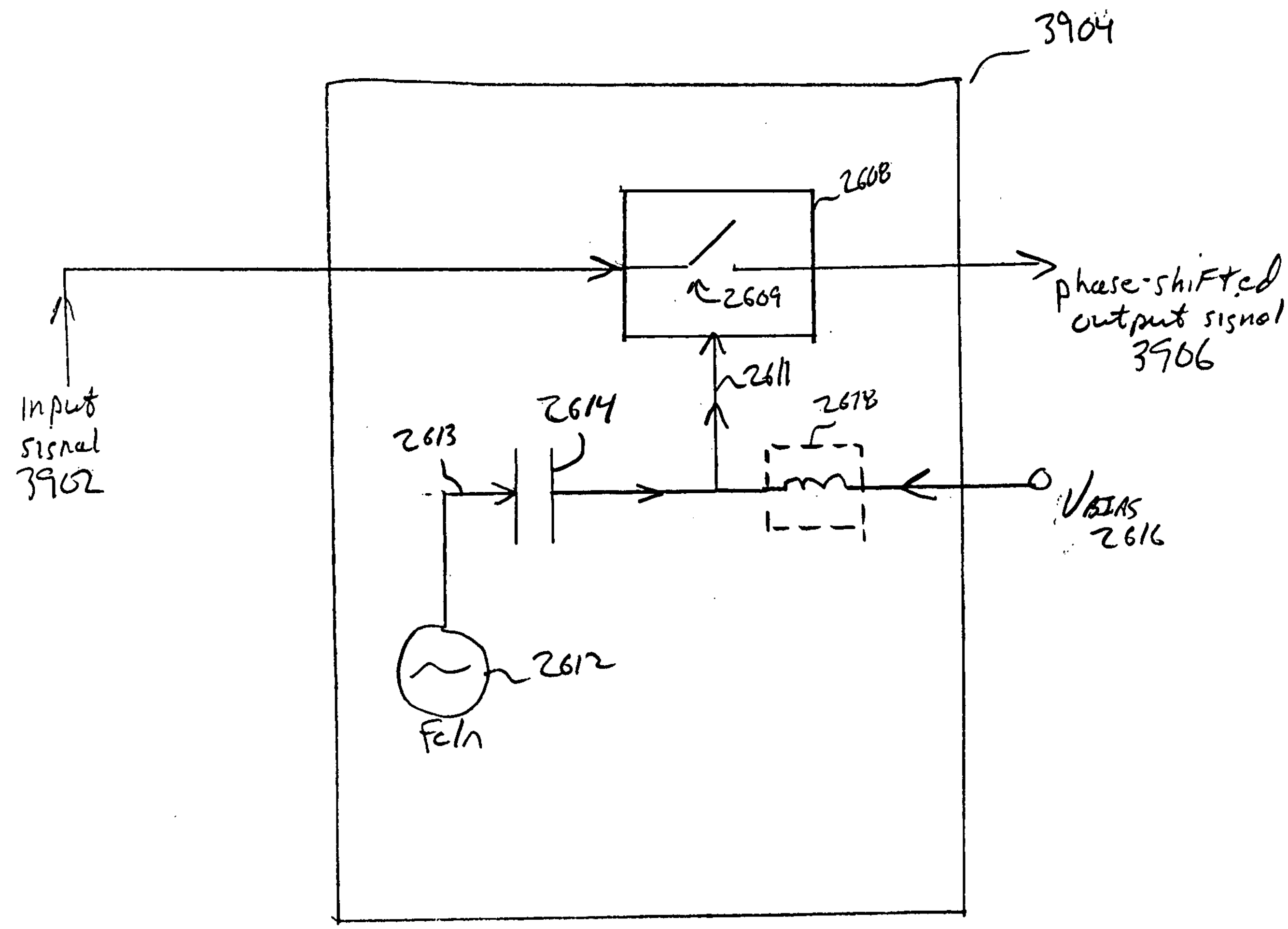

3904
2608
2609
phase-shifted output signal 3906
input signal 3902
2611
2618
2614
2613
VBIAS 2616
2612
Fc/n

FIG. 39

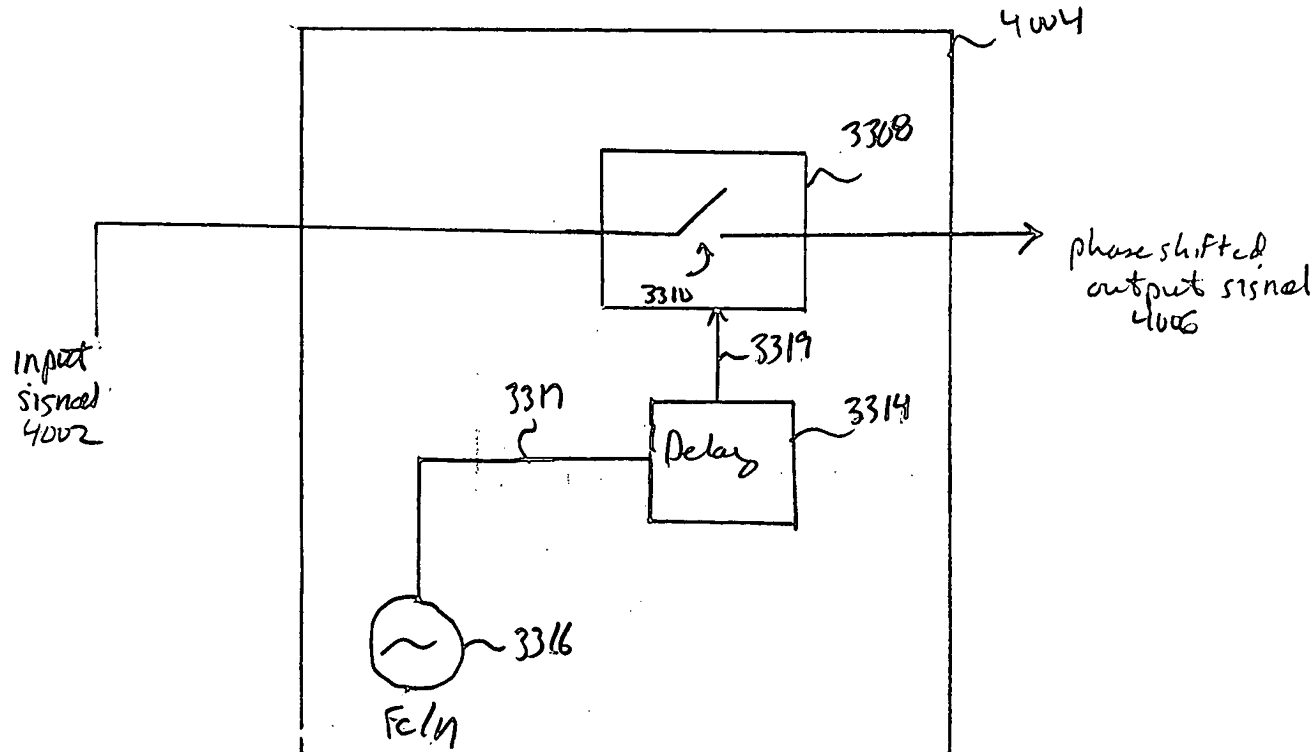

4004
3308
3310
3319
3314
Delay
3317
3316
Fc/N
input signal 4002
phase shifted output signal 4006

FIG. 40

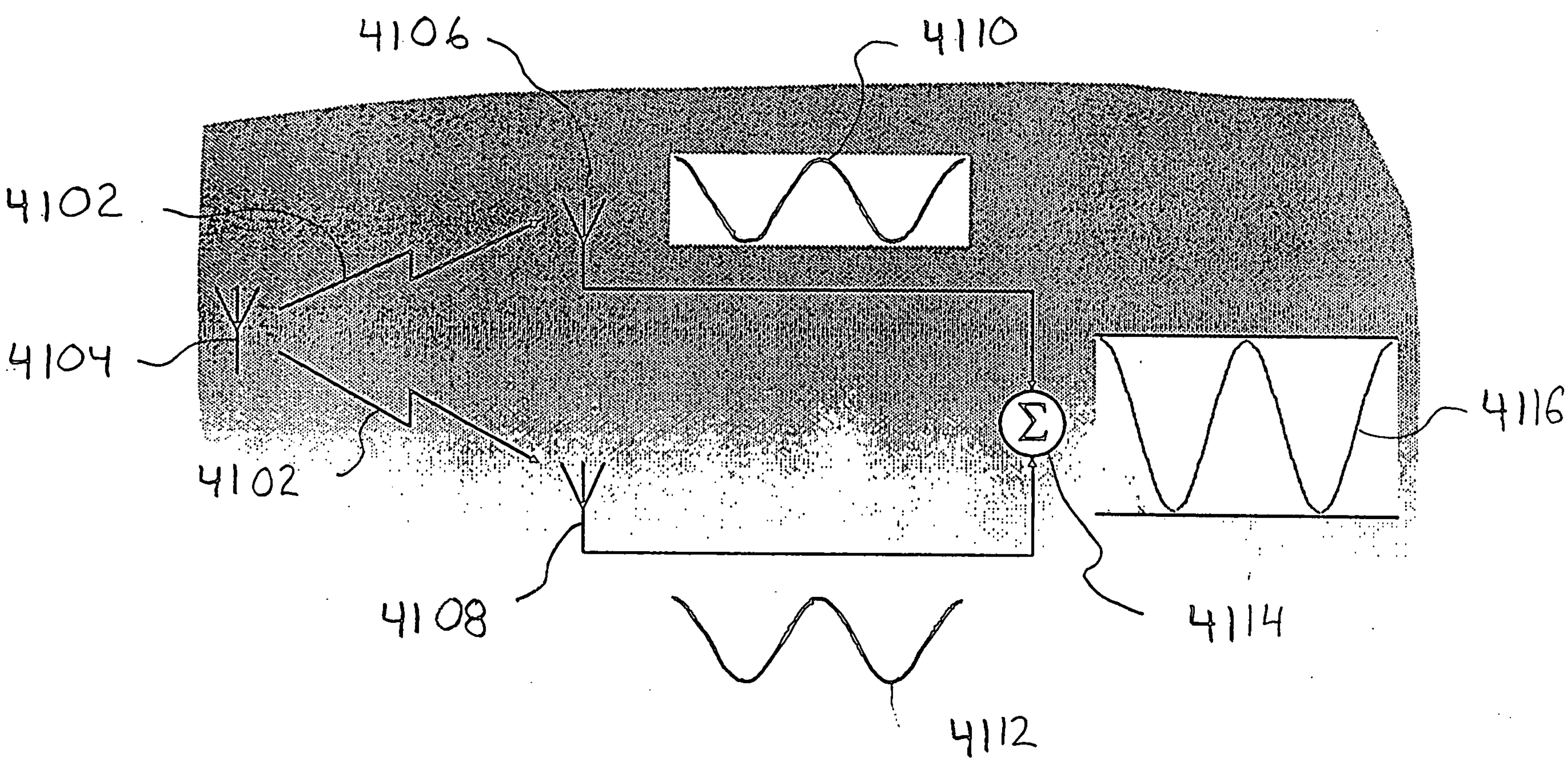


FIG. 41

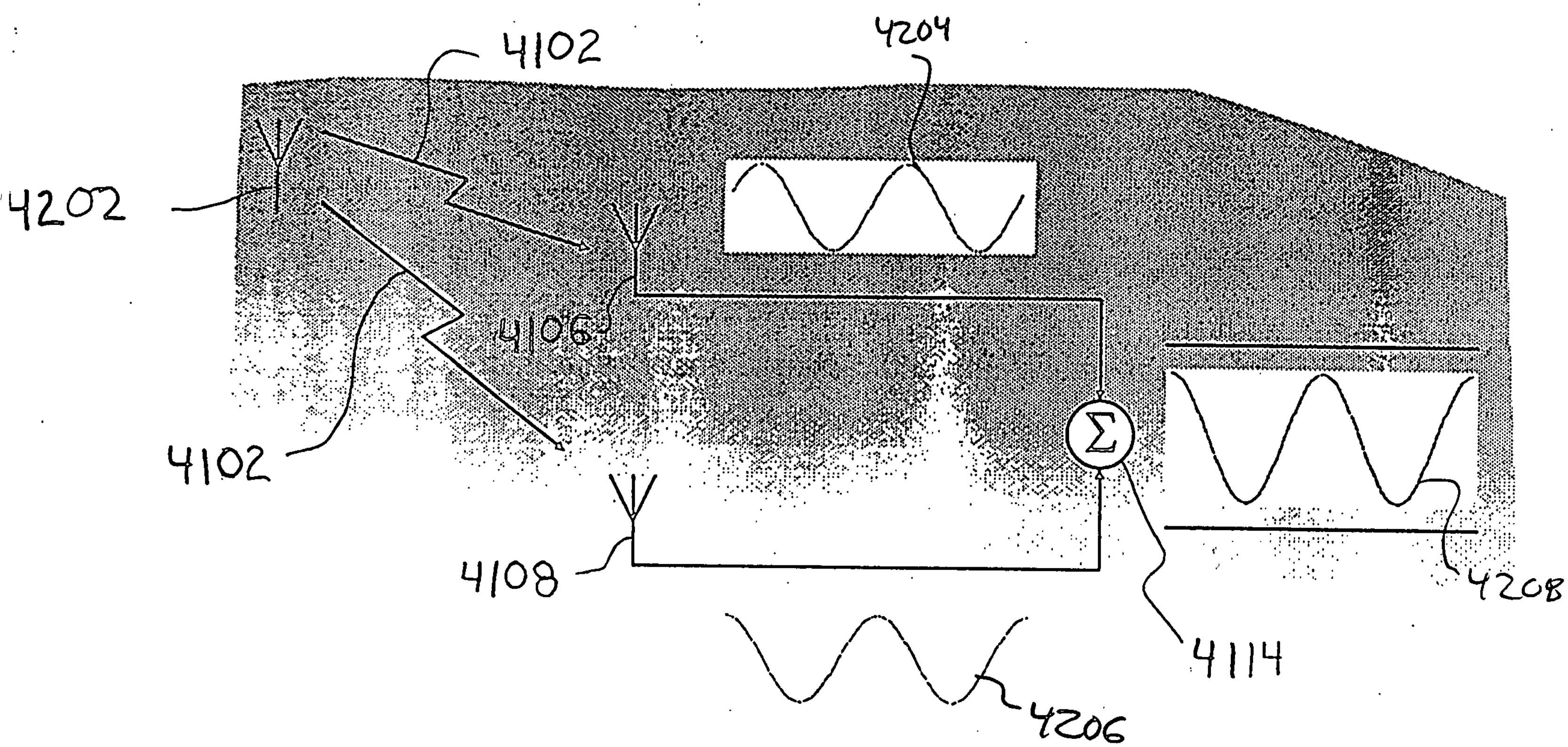


FIG. 42

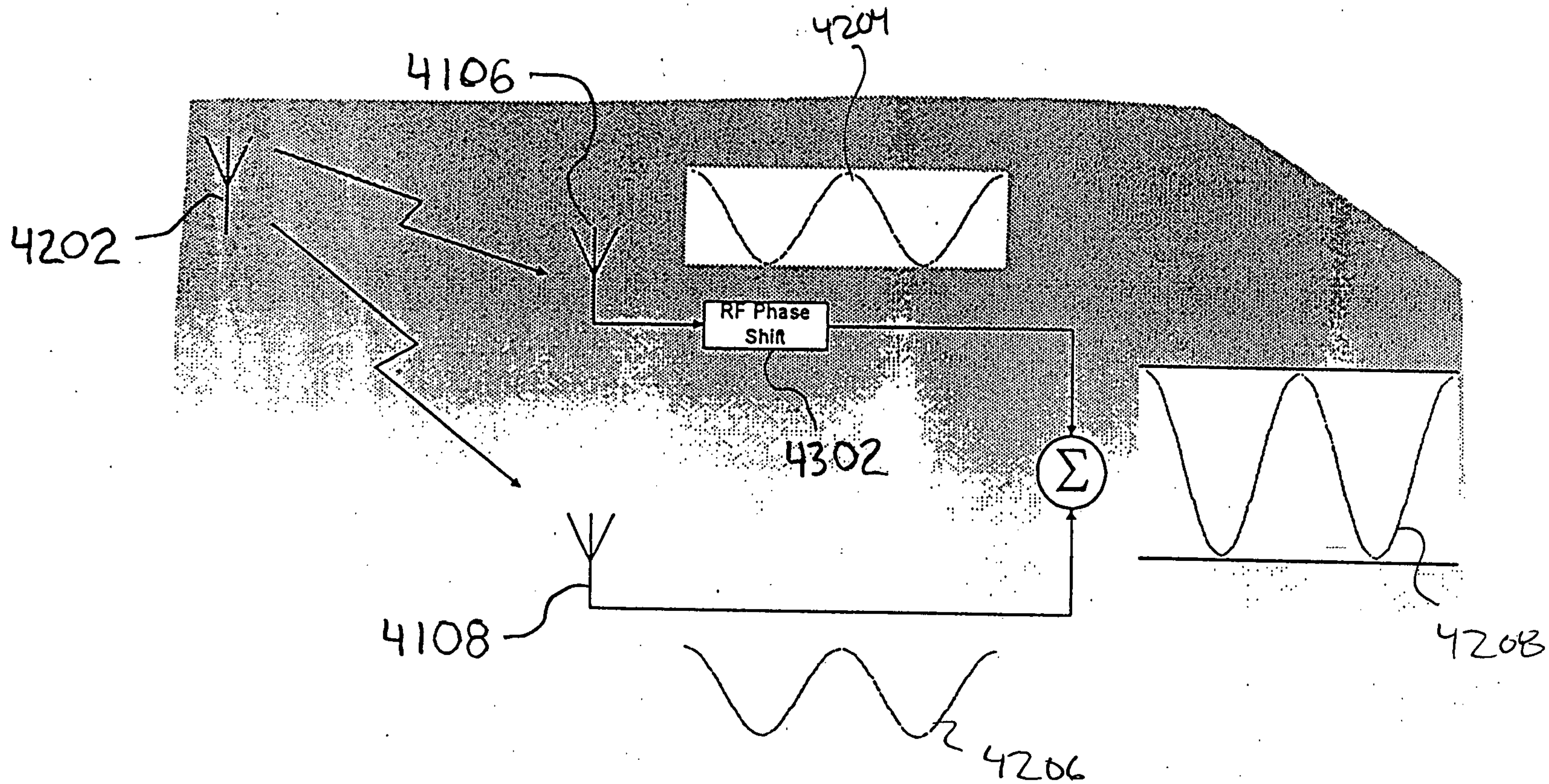


FIG. 43

No RF Phase Shift

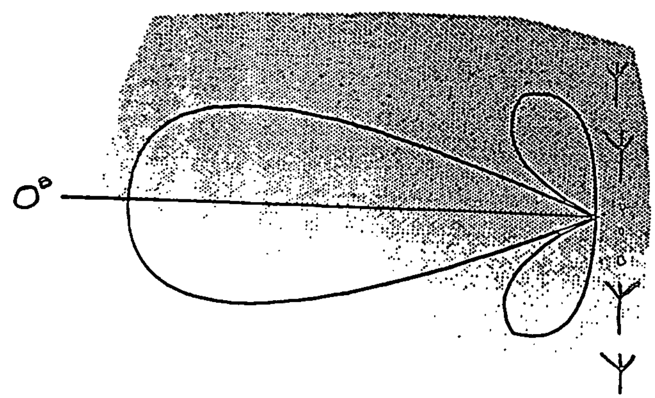


FIG. 44A

RF Phase Shift

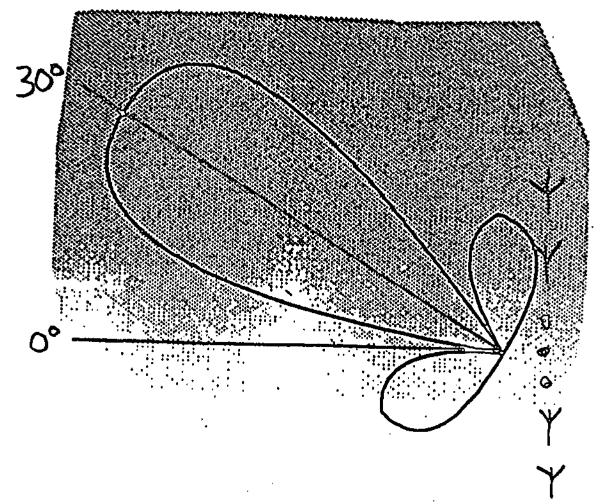


FIG. 44B

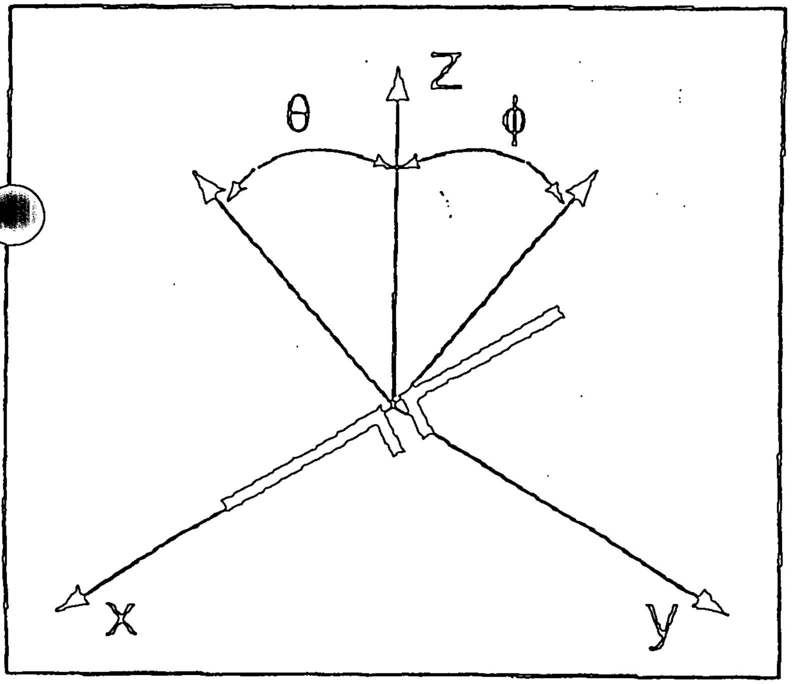


FIG. 45A *Half-wave dipole*

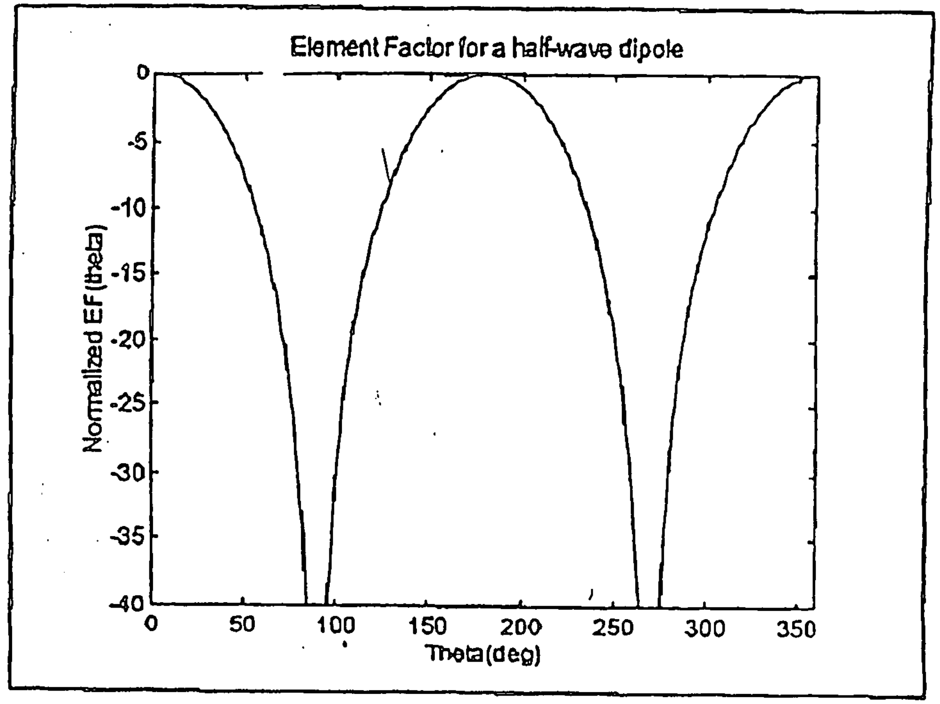


FIG. 45B *E-plane element factor for a half-wave dipole.*

09590955.060900

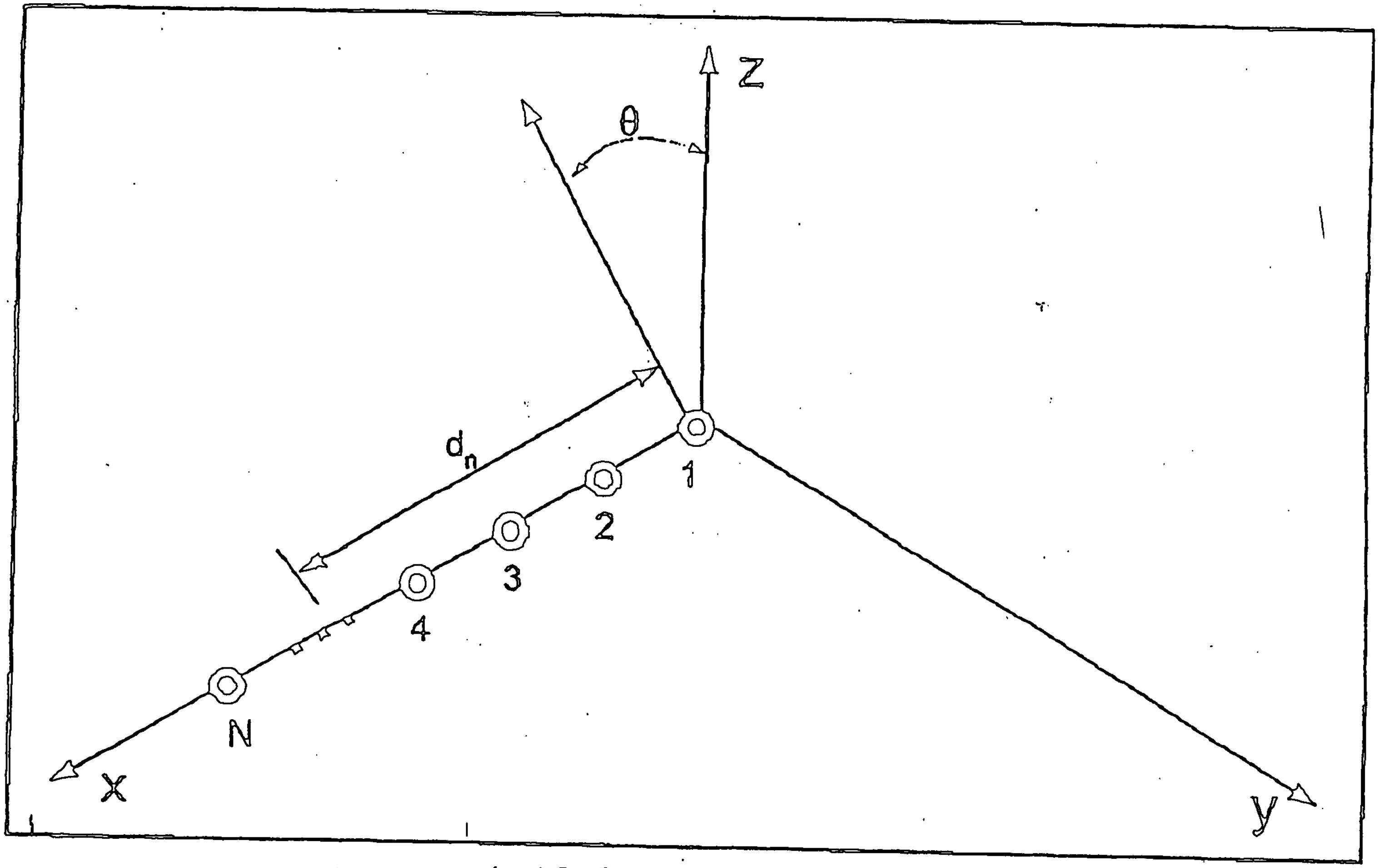


FIG. 46 *An N-element linear antenna array.*

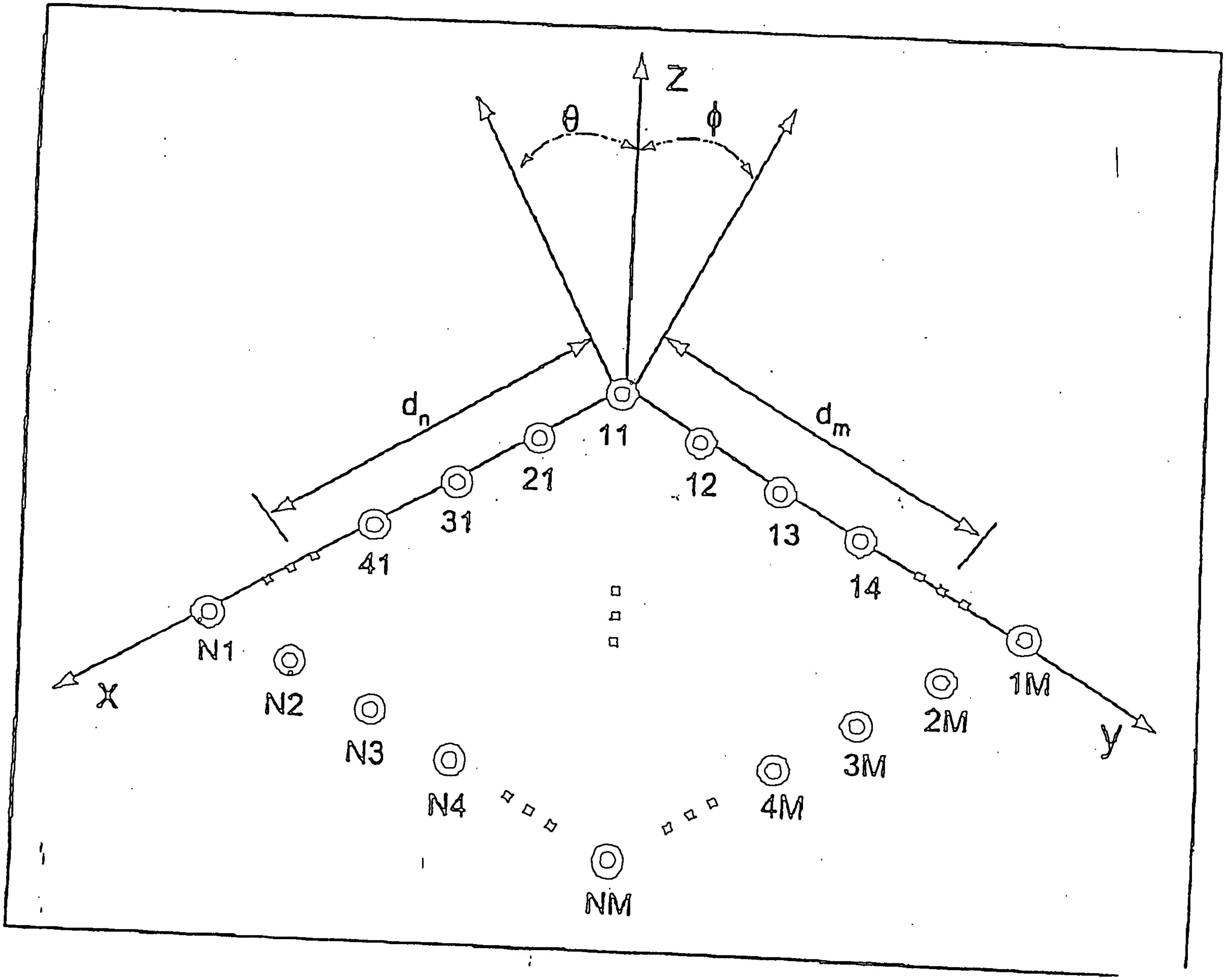


FIG. 47

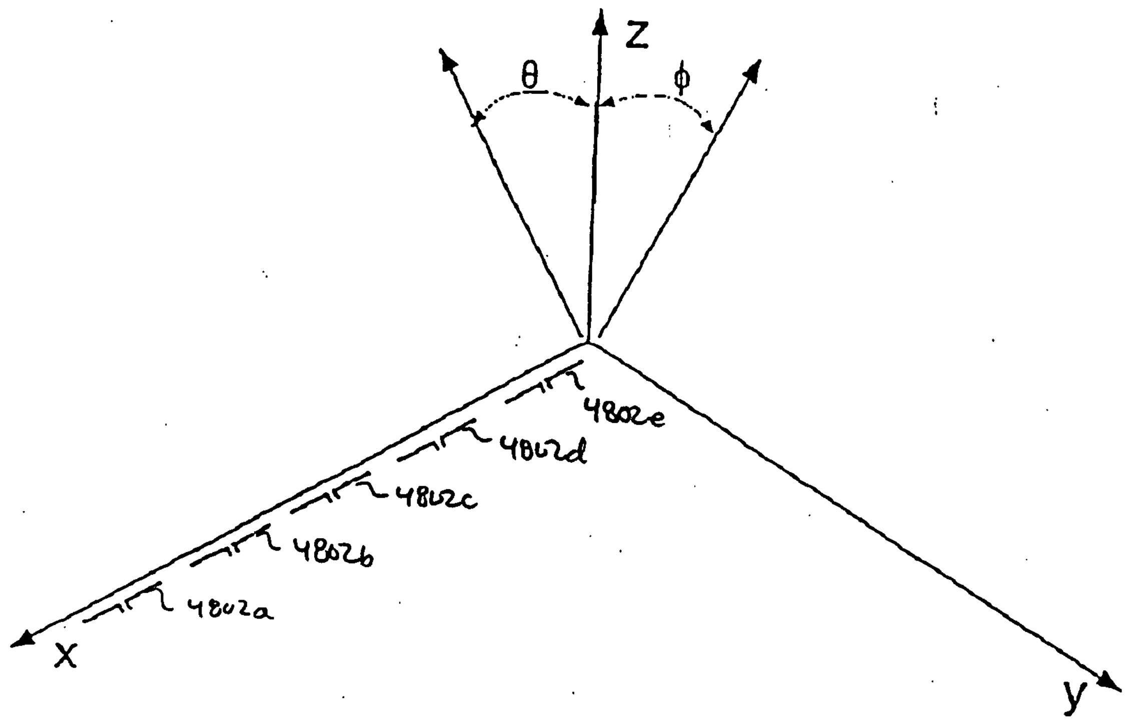
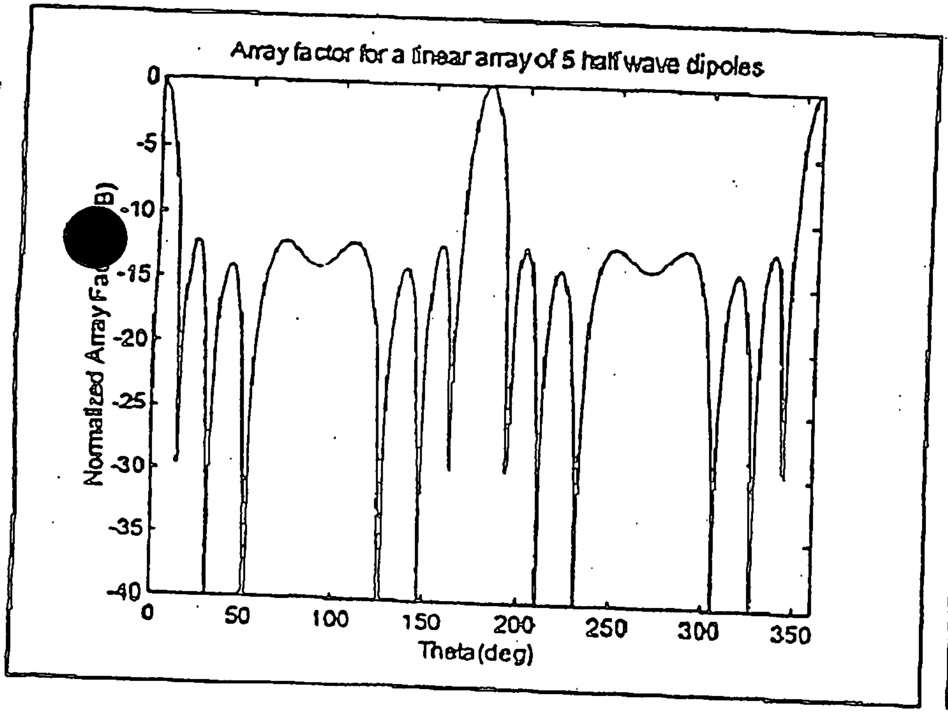


FIG. 48 *A linear array of five half wave dipoles.*



F[illegible] 49A *Array factor for the linear array.*

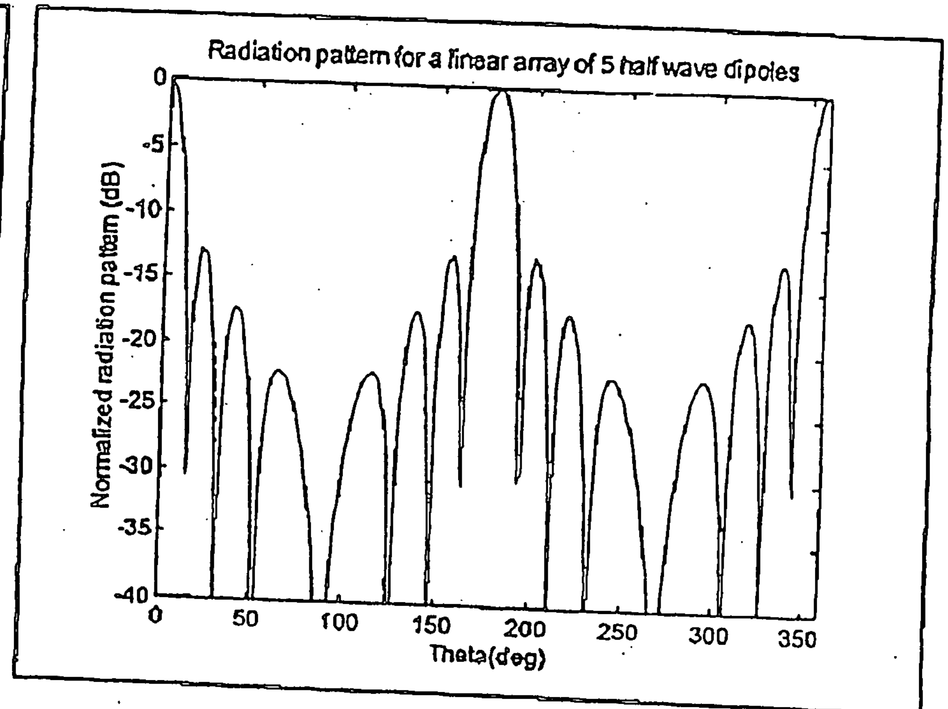


FIG.49B *Radiation pattern for the linear array.*

09590955 .060900

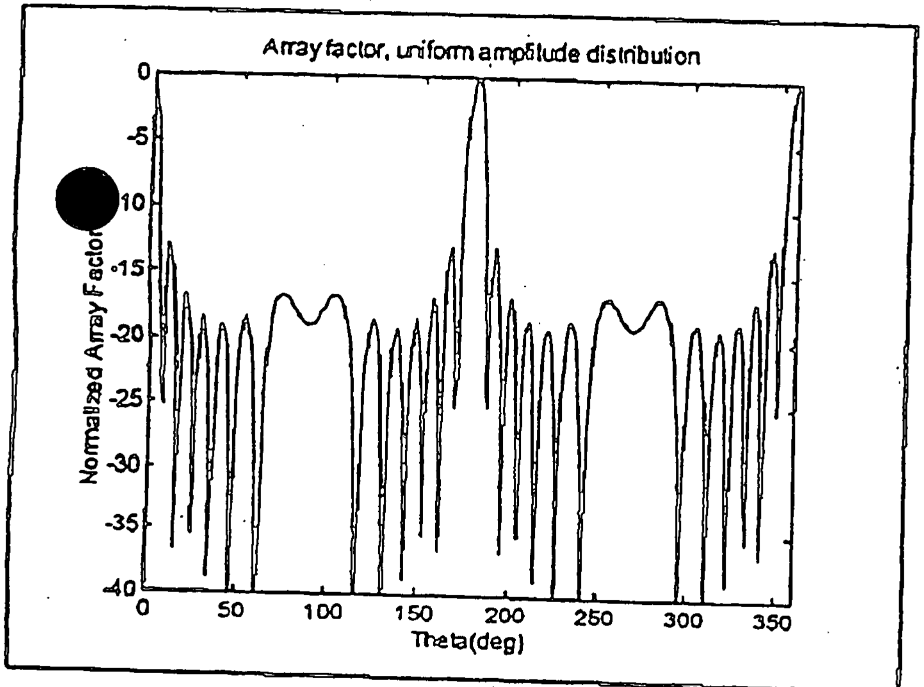


FIG. 50A *Array factor, uniform amplitude distribution*

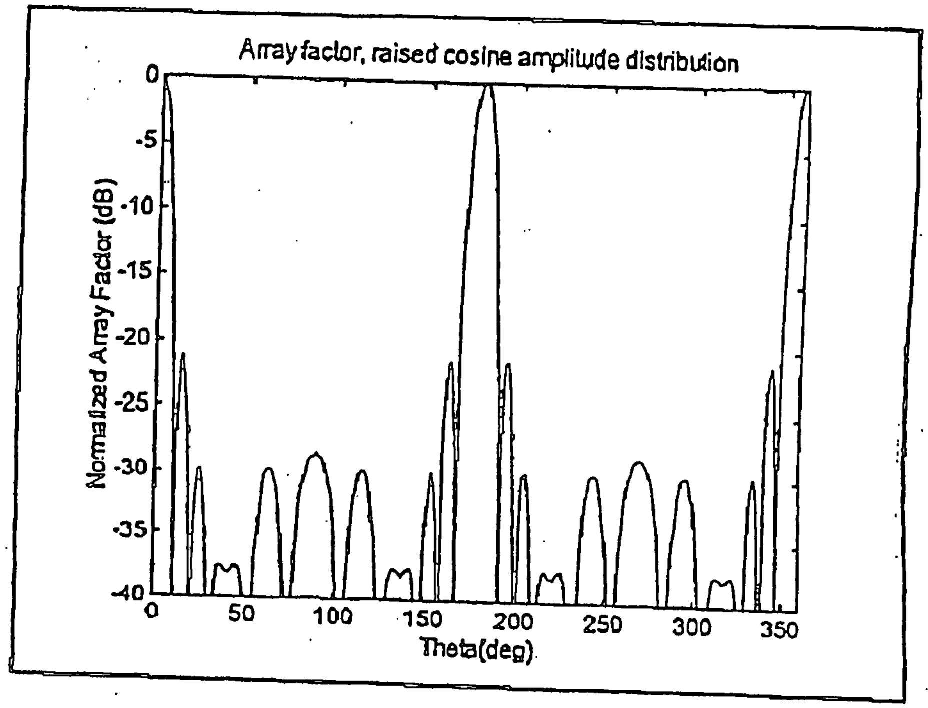


FIG. 50B *Array factor raised cosine amplitude distribution*

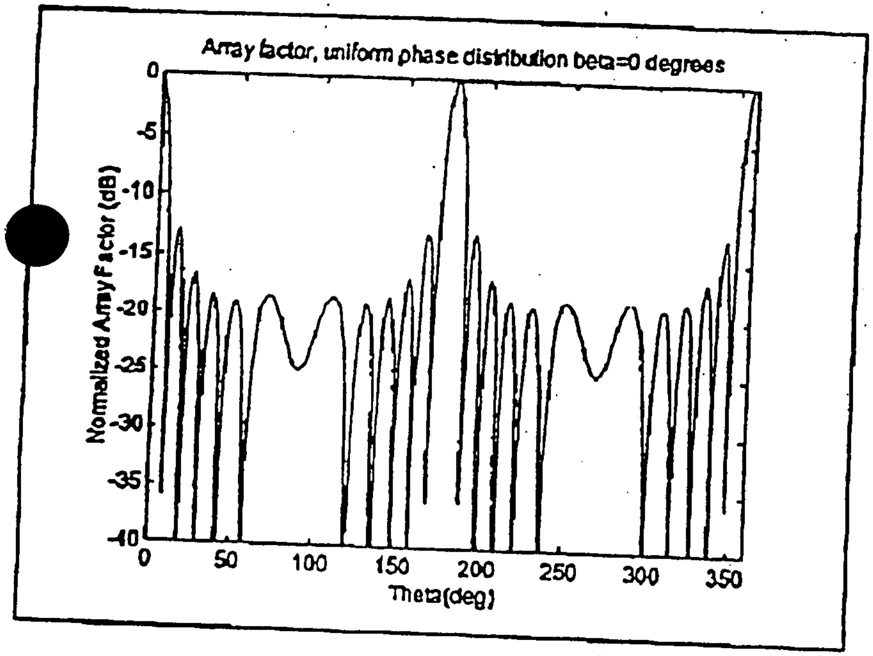


FIG. 51A *Array factor, uniform phase distribution*

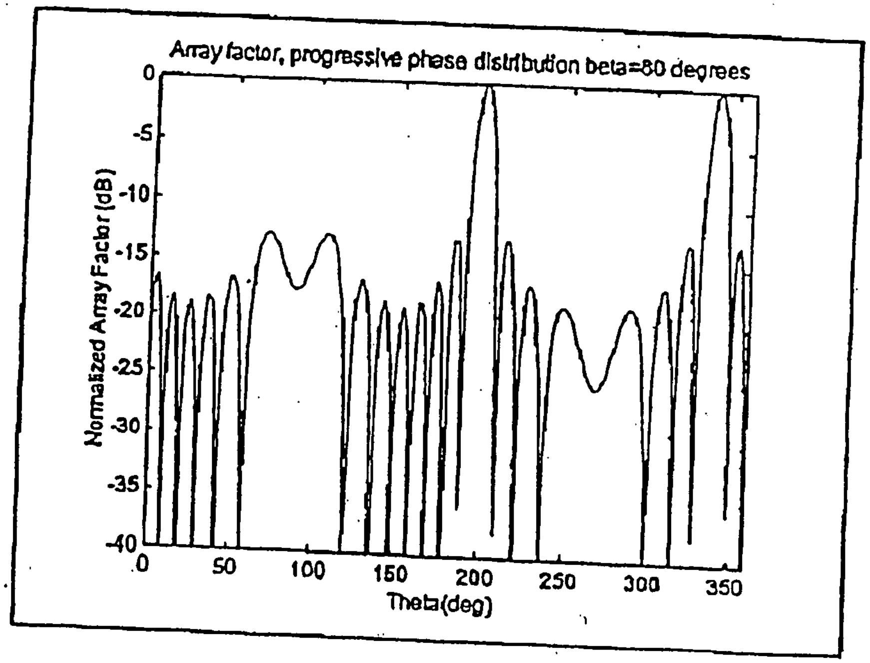


FIG. 51B *Array factor progressive phase distribution*

006090"SS606S60

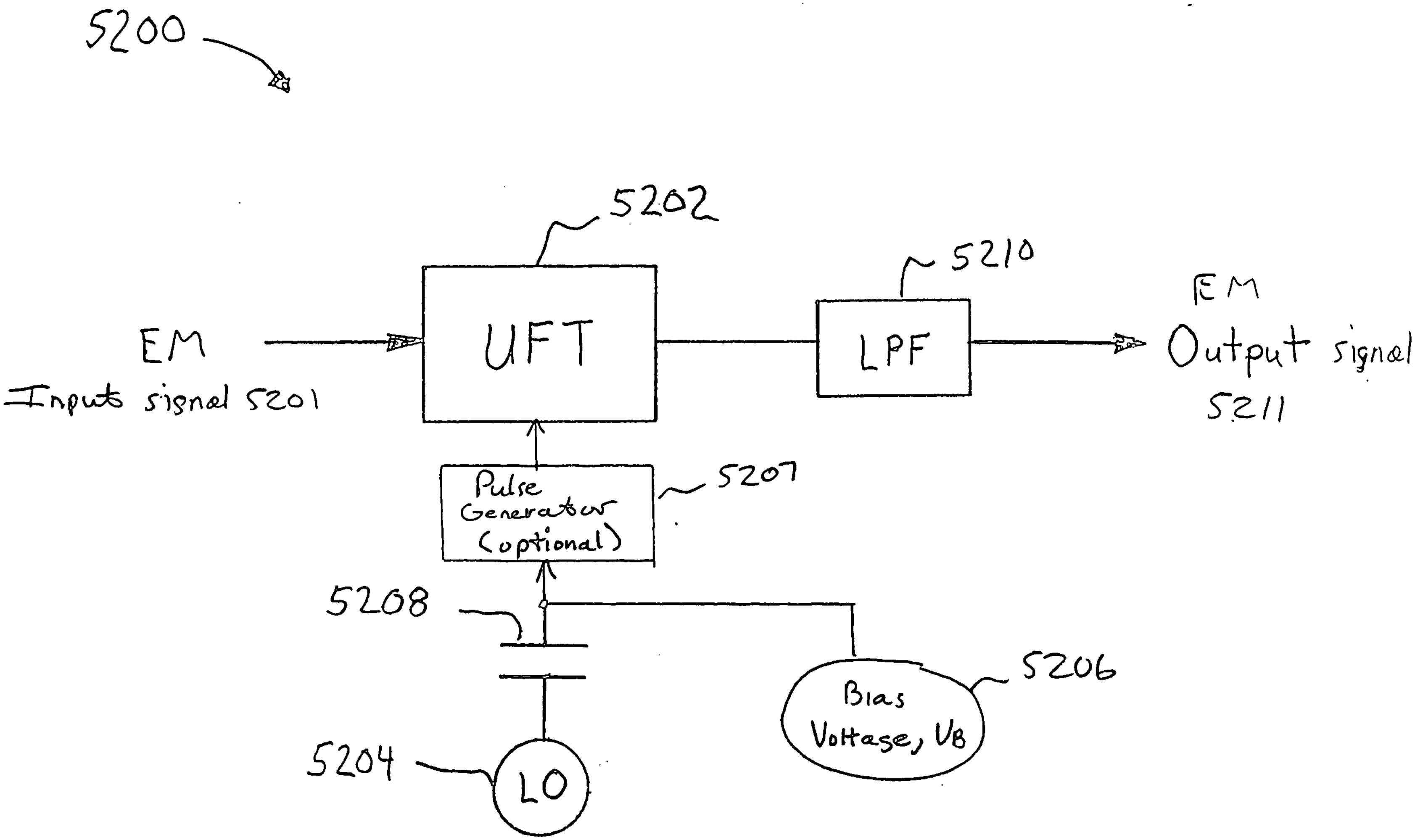


FIG. 52

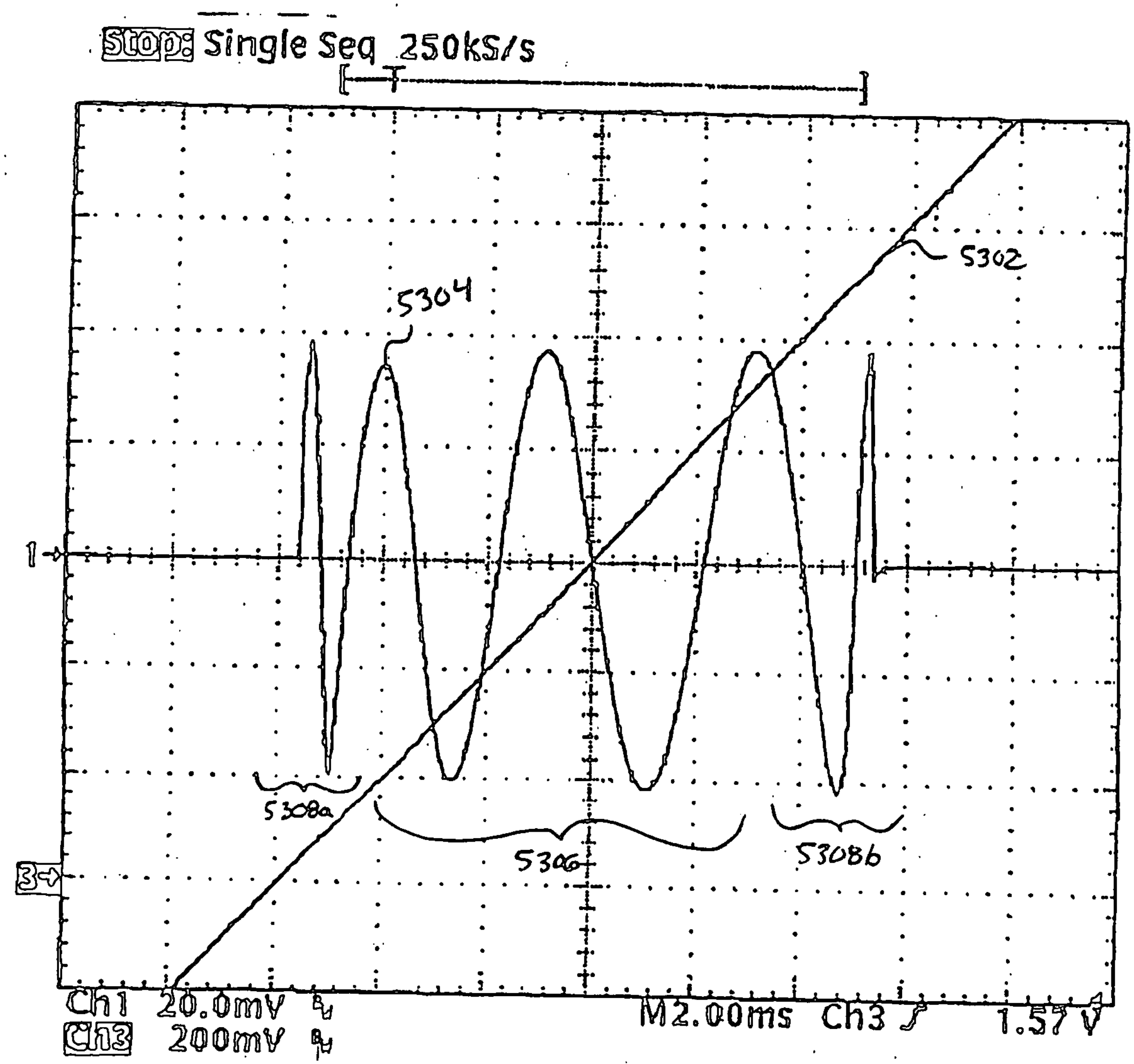

Stop: Single Seq 250kS/s
5302
5304
5308a
5306
5308b
1
3
Ch1 20.0mV
Ch3 200mV
M2.00ms Ch3
1.57 V

FIG. 53

Range of Valid Bias Voltages vs. LO Amplitude for V_{cc}=5 VDC

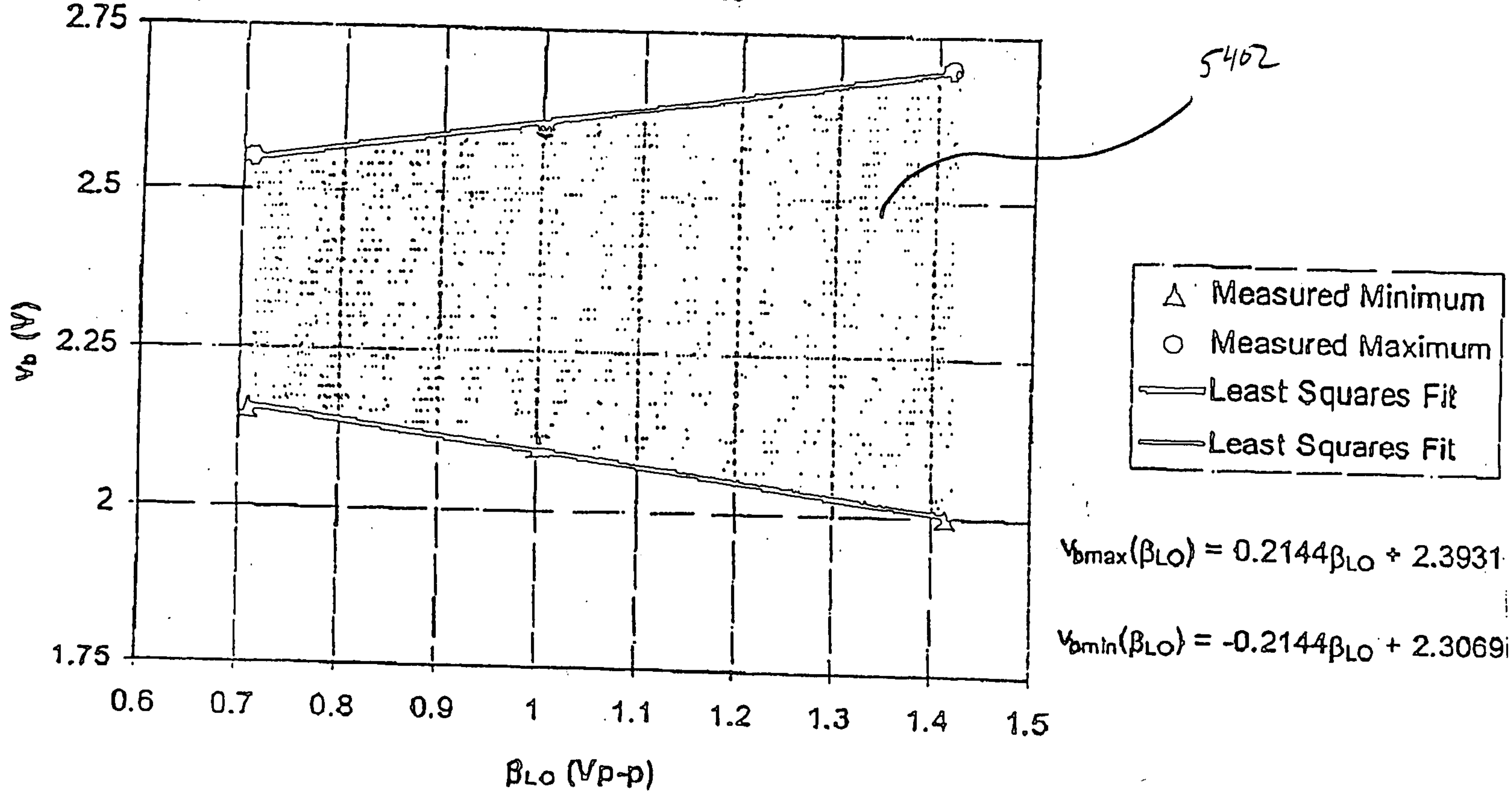
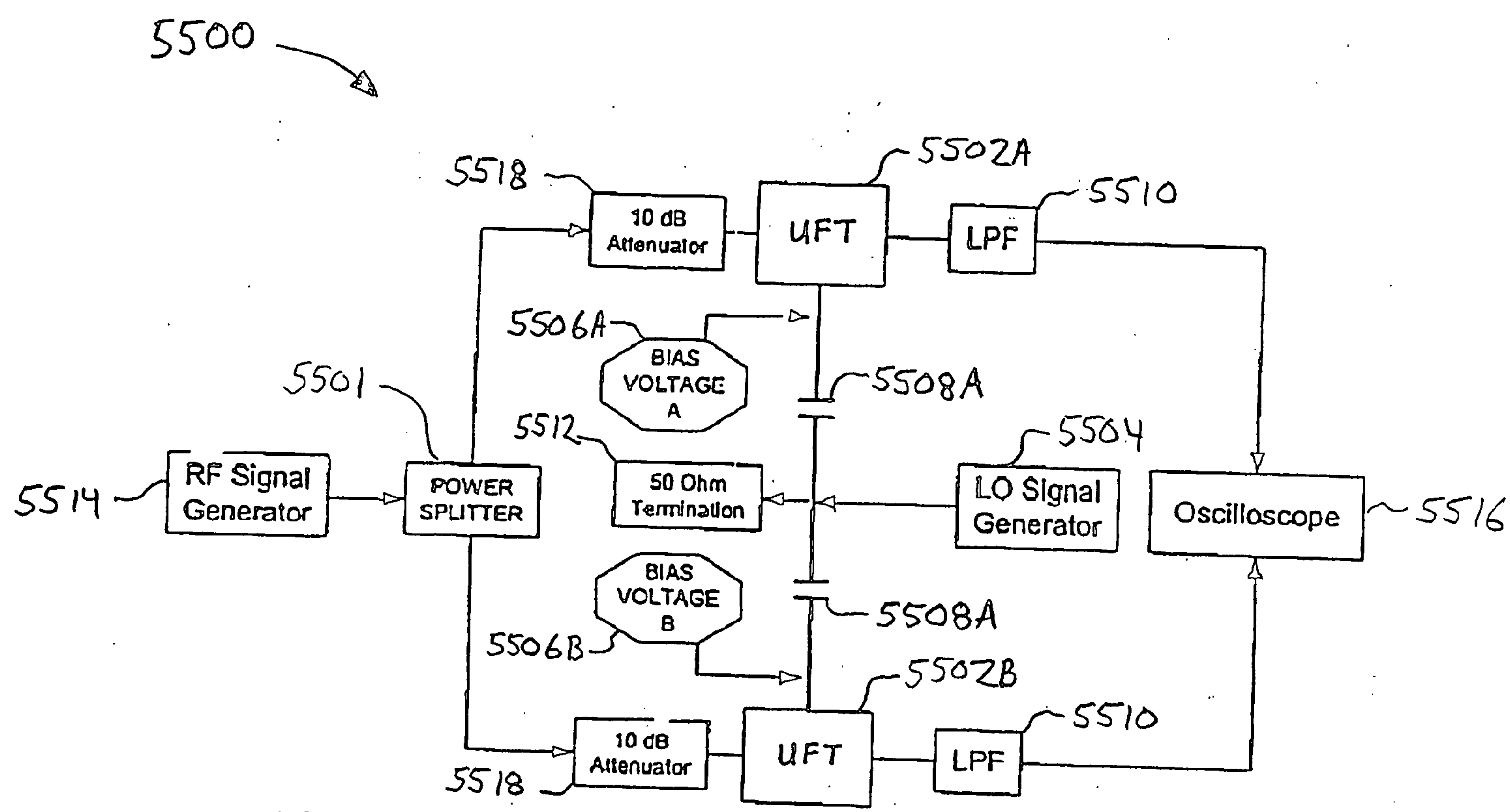
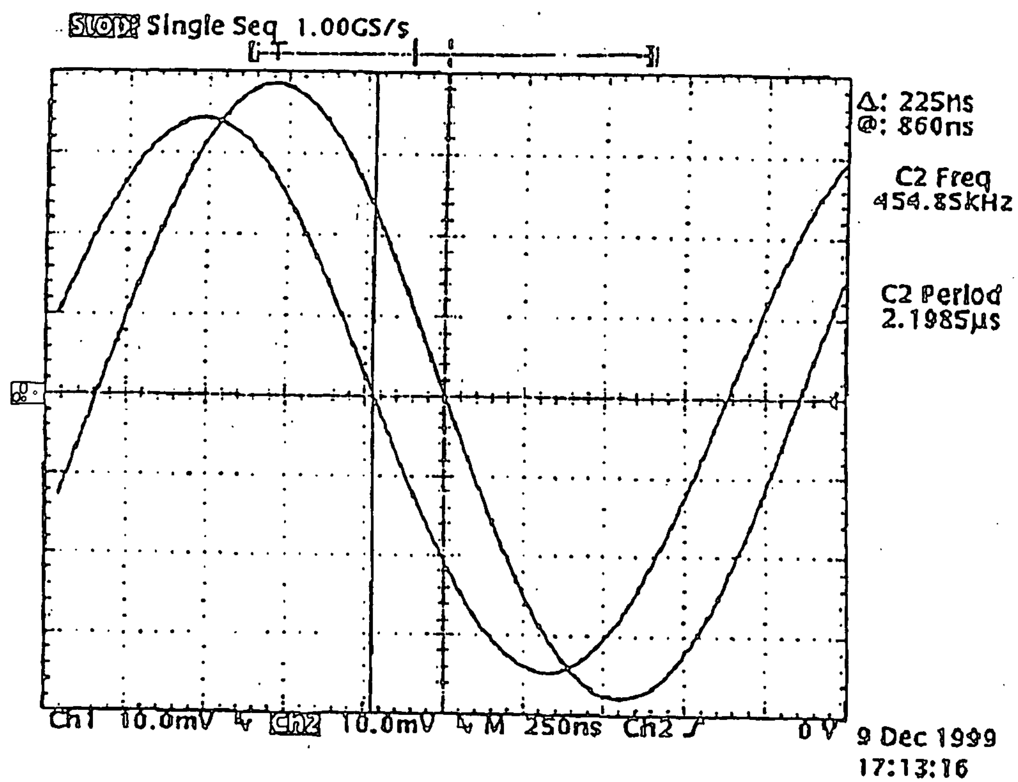


FIG. 54



A block diagram of a circuit where the phase of the two outputs can be adjusted independently by setting the LO bias voltages.

FIG. 55



Measured phase shift for the design example.

FIG. 56

Measured and Approximated UFT Phase Function for p-p LO Amplitude of 7 dBm in to 50 ohms.

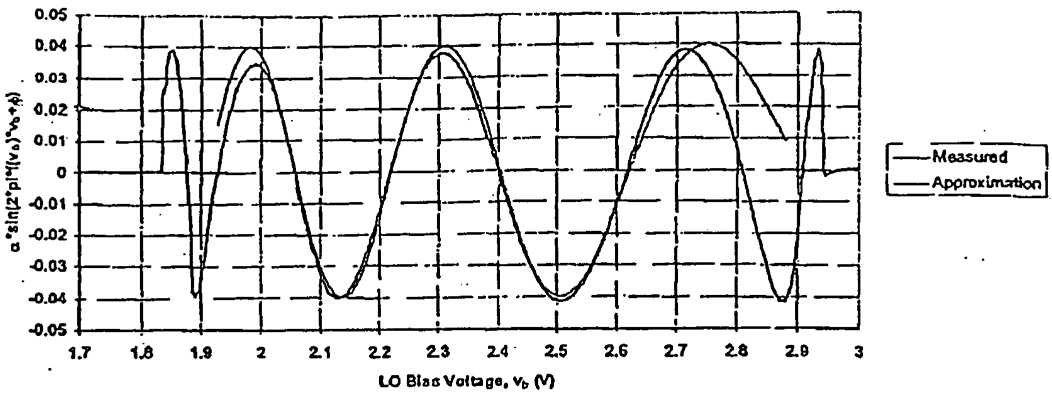


FIG. 57A

Measured and Approximated UFT Phase Function for p-p LO Amplitude of 4 dBm in to 50 ohms.

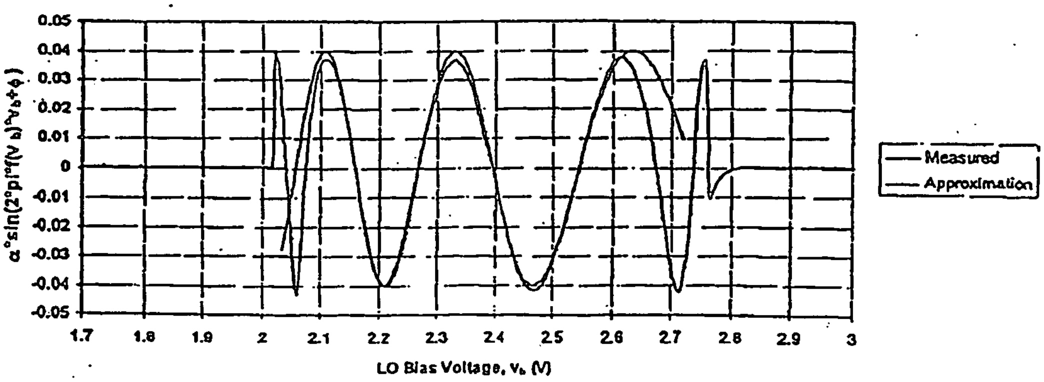


FIG. 57B

Measured and Approximated UFT Phase Function for p-p LO Amplitude of 1 dBm in to 50 ohms.

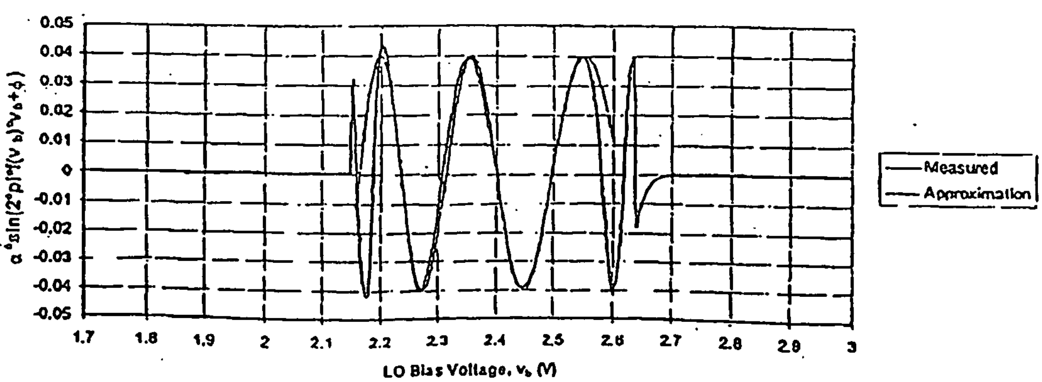


FIG. 57C

ϕ

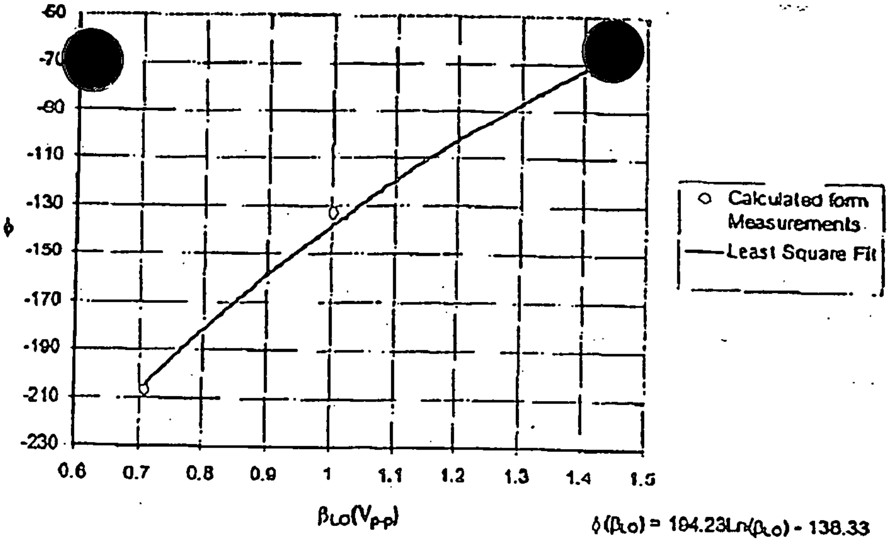


FIG. 58A

f_o

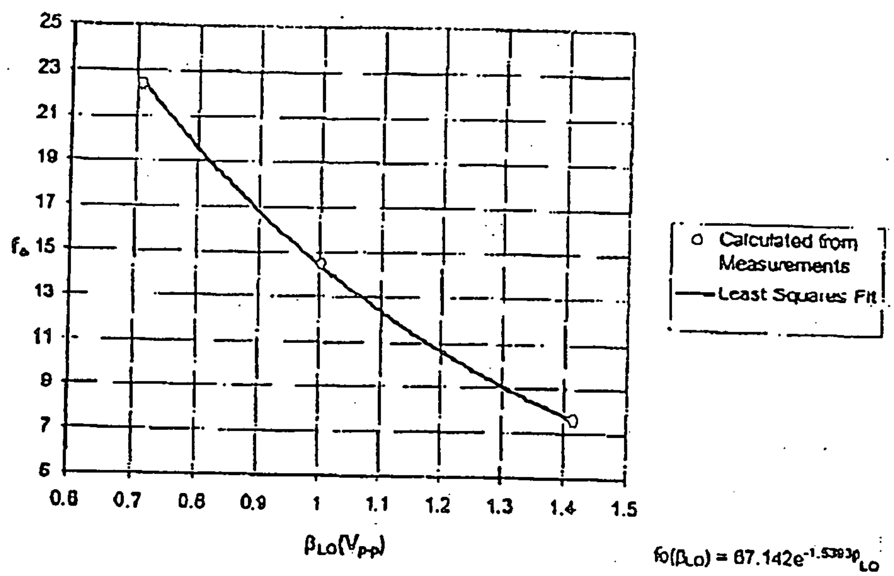


FIG. 58B

ρ

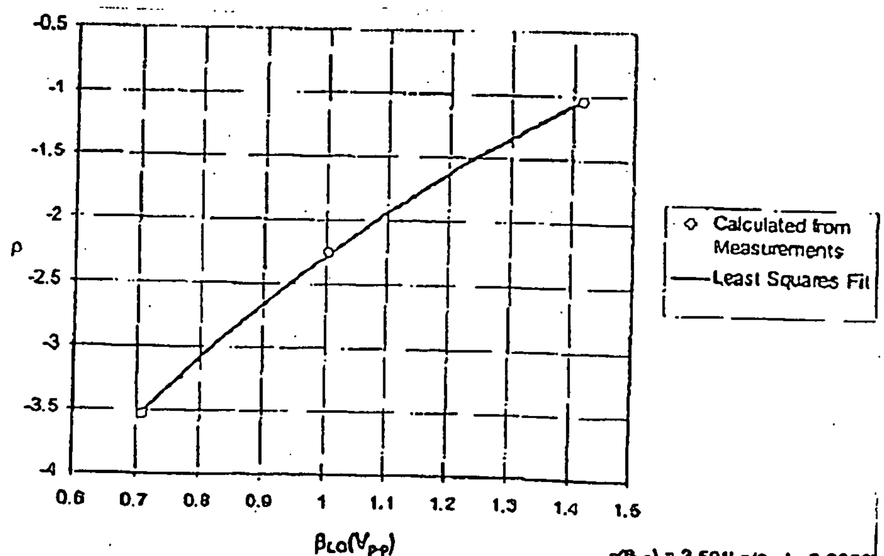


FIG. 58C

00609O"5S606S60

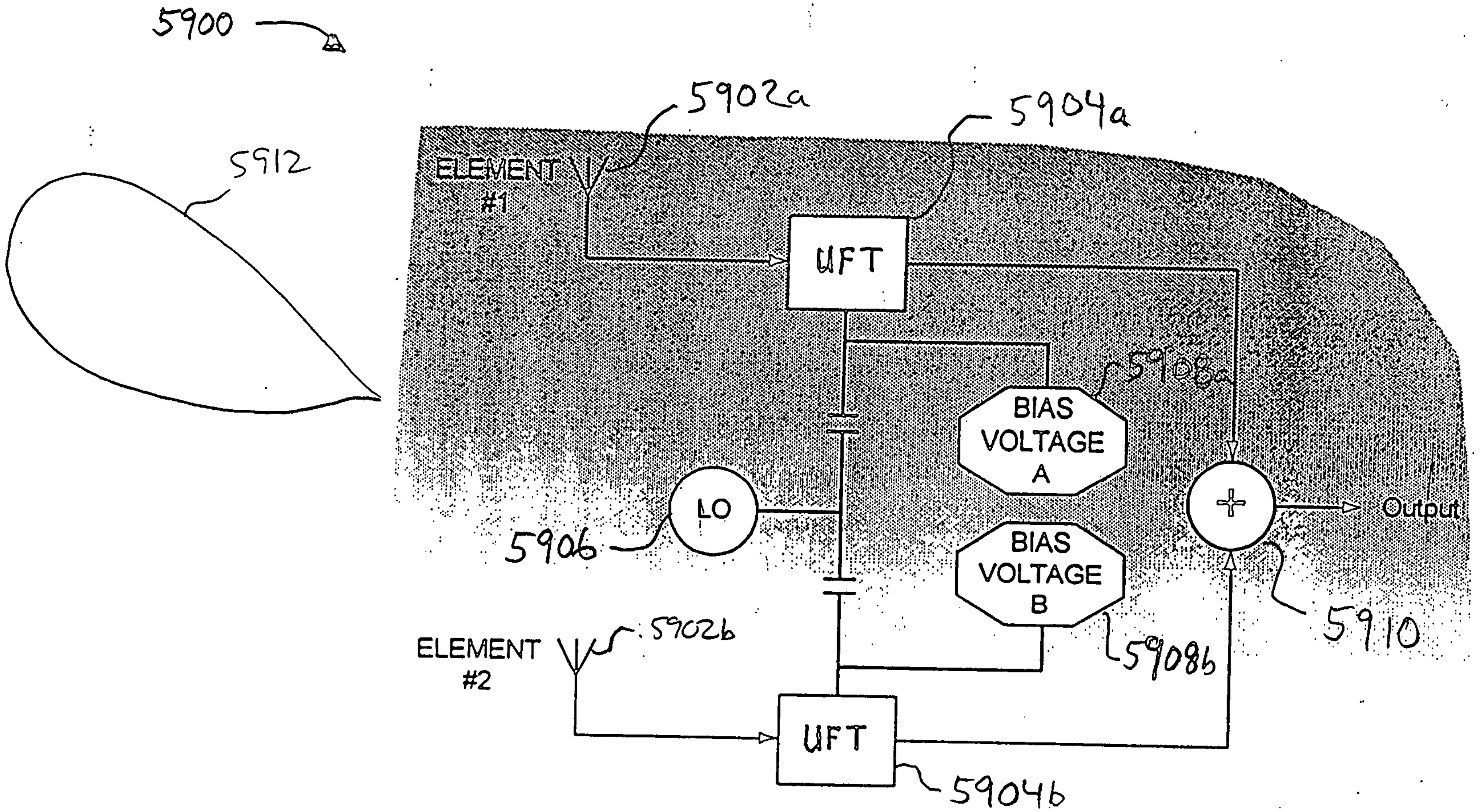


FIG. 59

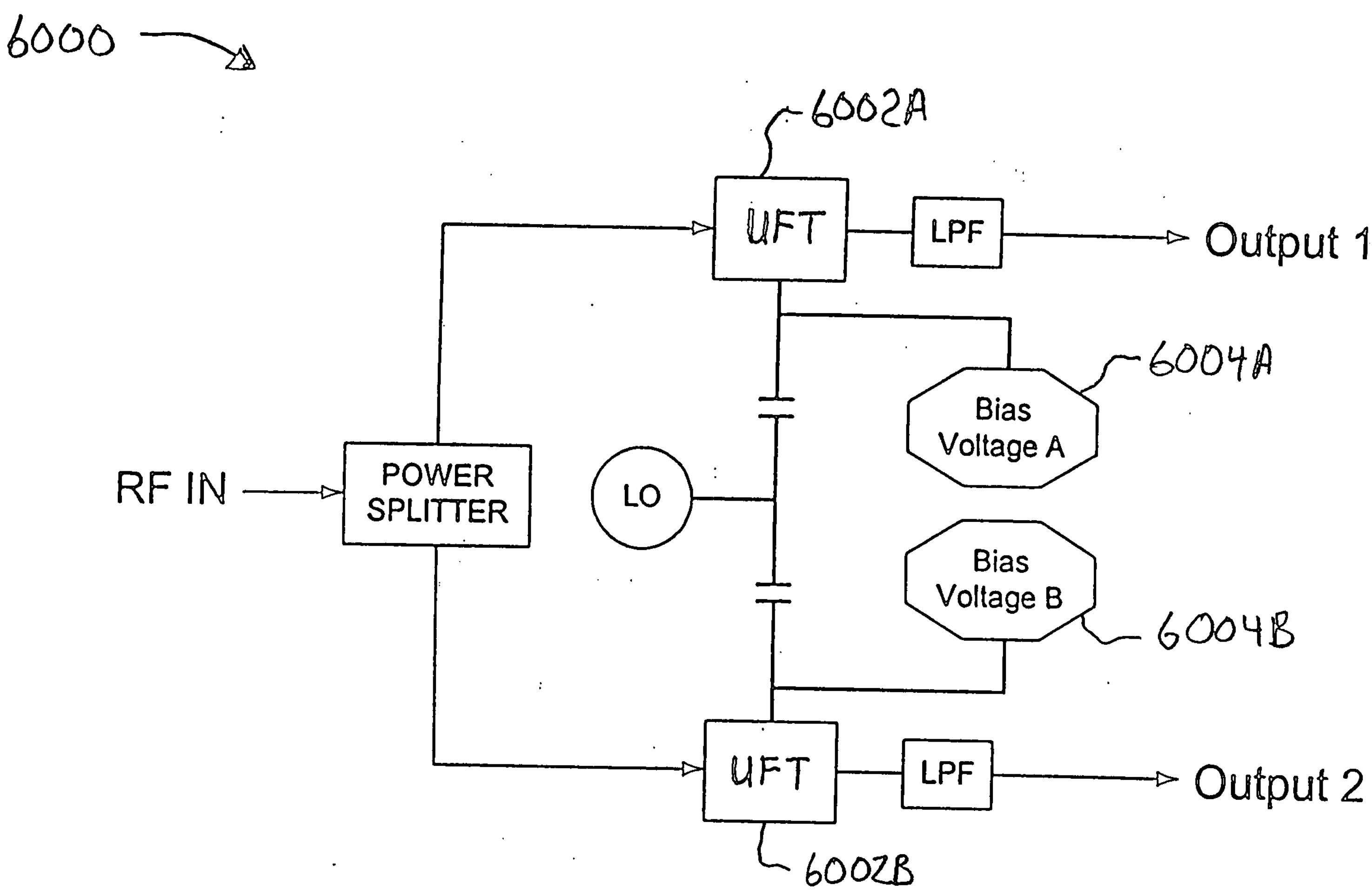

6000
6002A
UFT
LPF
Output 1
6004A
Bias Voltage A
RF IN
POWER SPLITTER
LO
Bias Voltage B
6004B
UFT
LPF
Output 2
6002B

FIG. 60

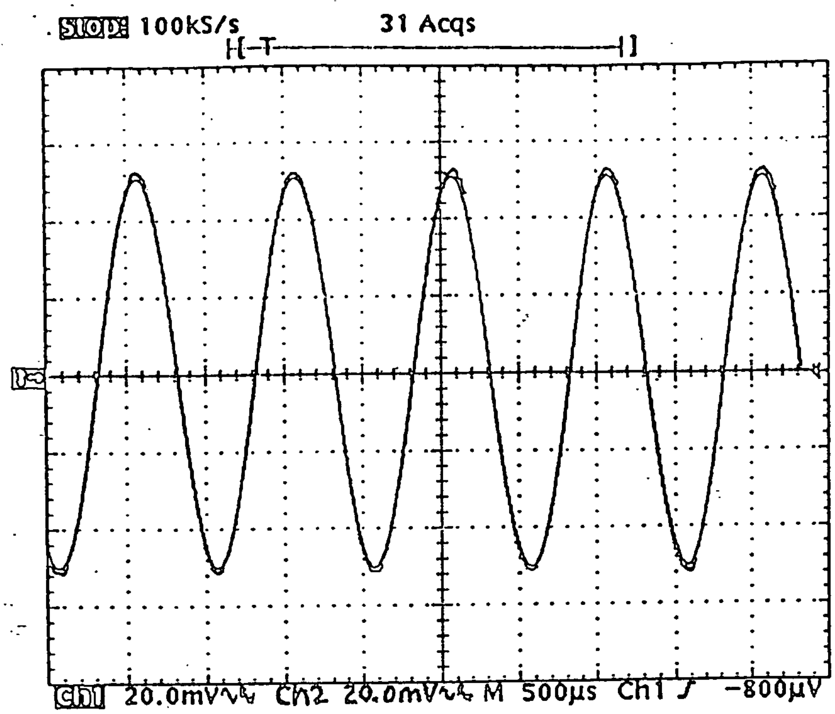


FIG. 61A

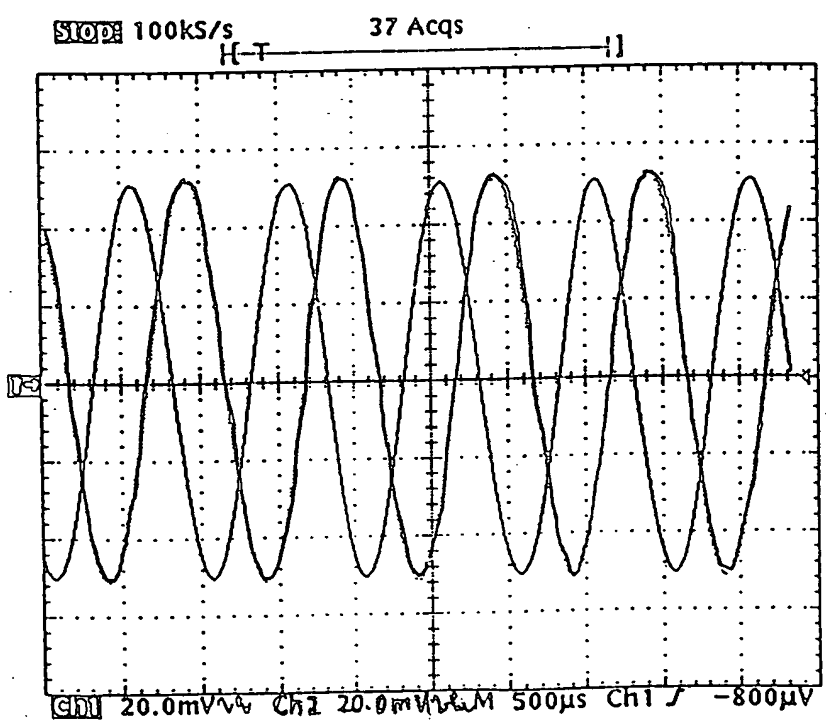
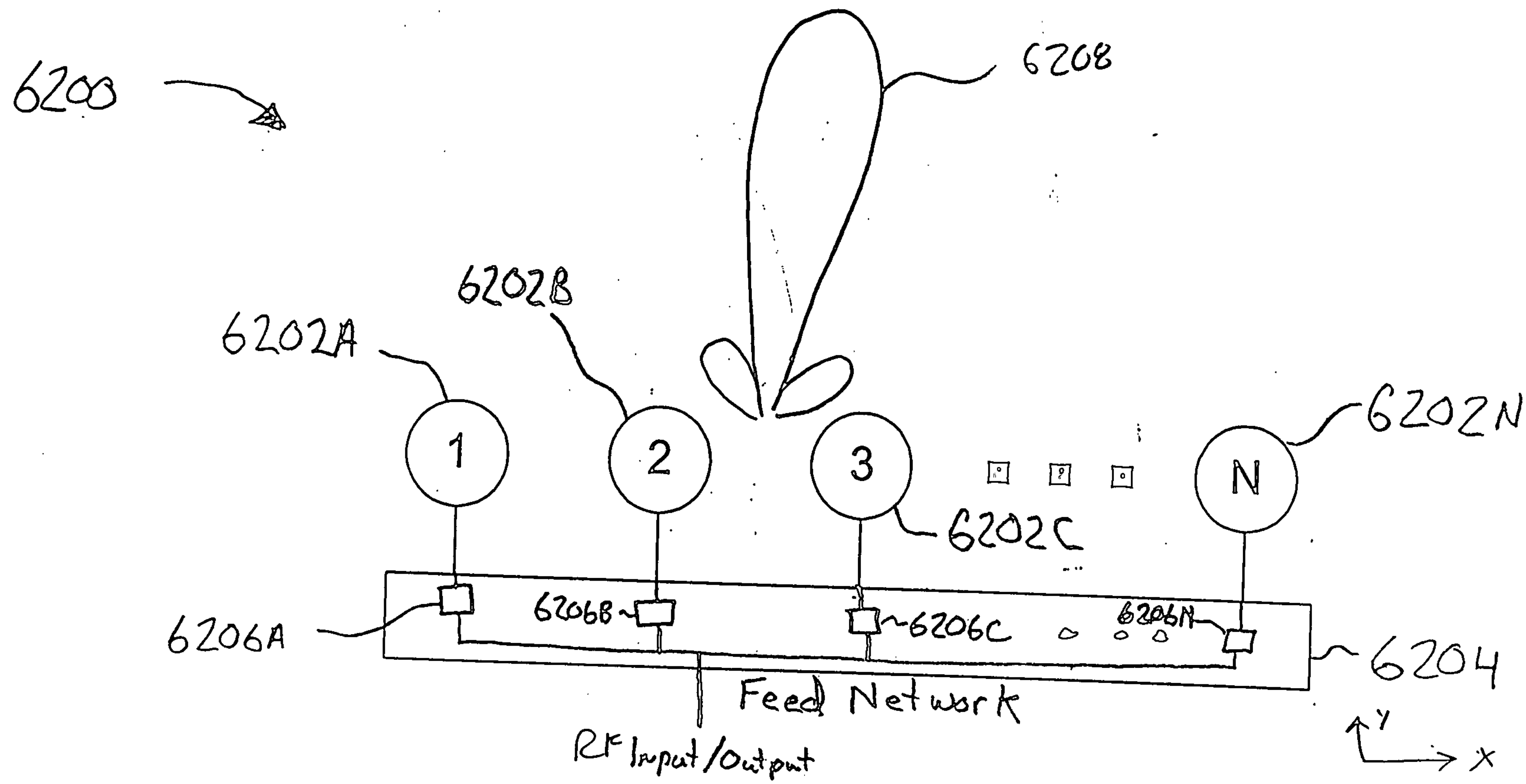


FIG. 61B



6200
6208
6202A
6202B
6202C
6202N
1
2
3
N
6206A
6206B
6206C
6206N
6204
Feed Network
RF Input/Output
Y
X

FIG. 62

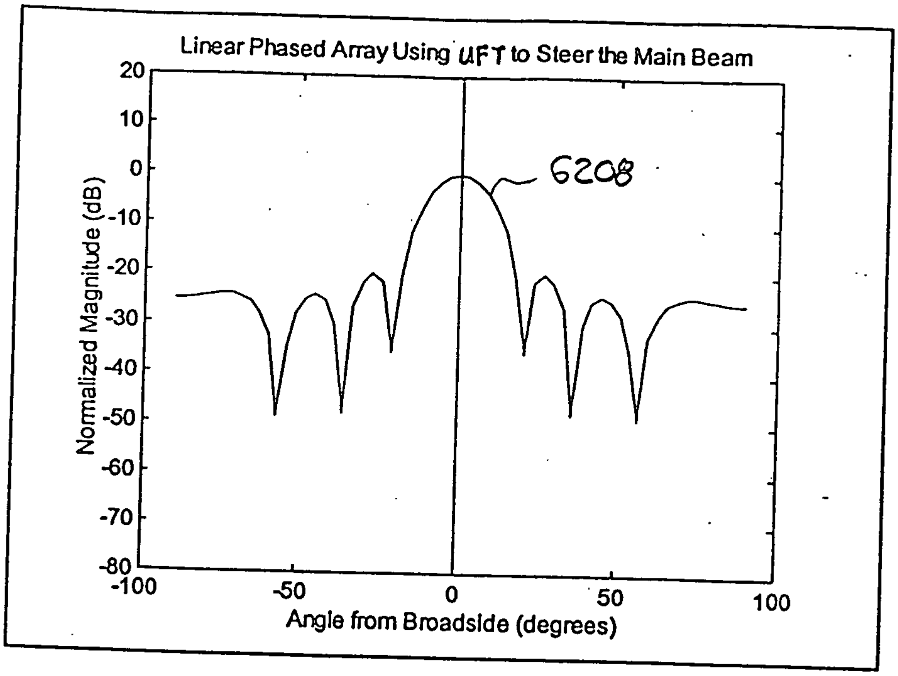


FIG. 63A

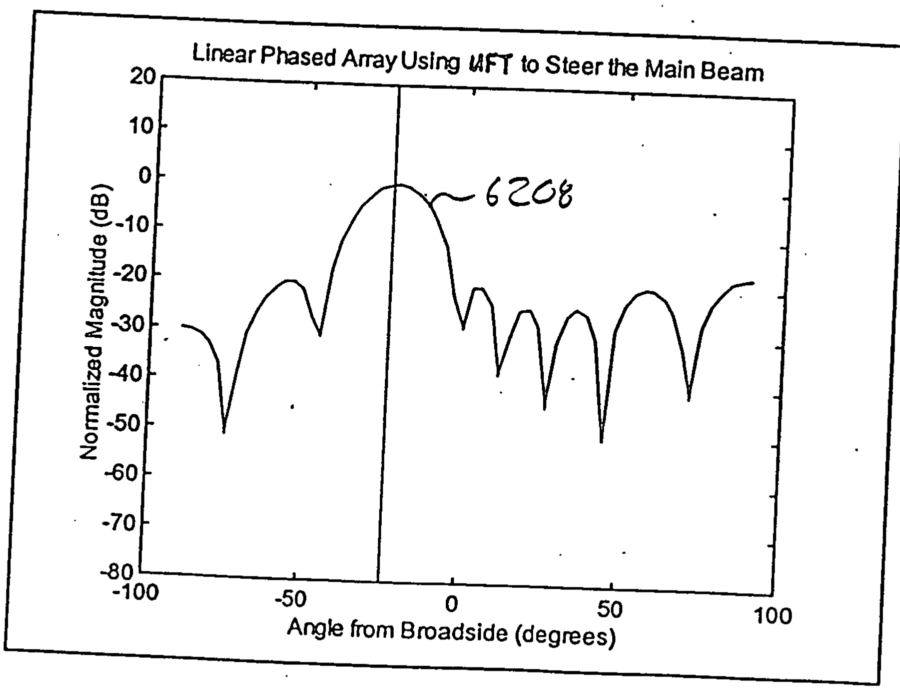
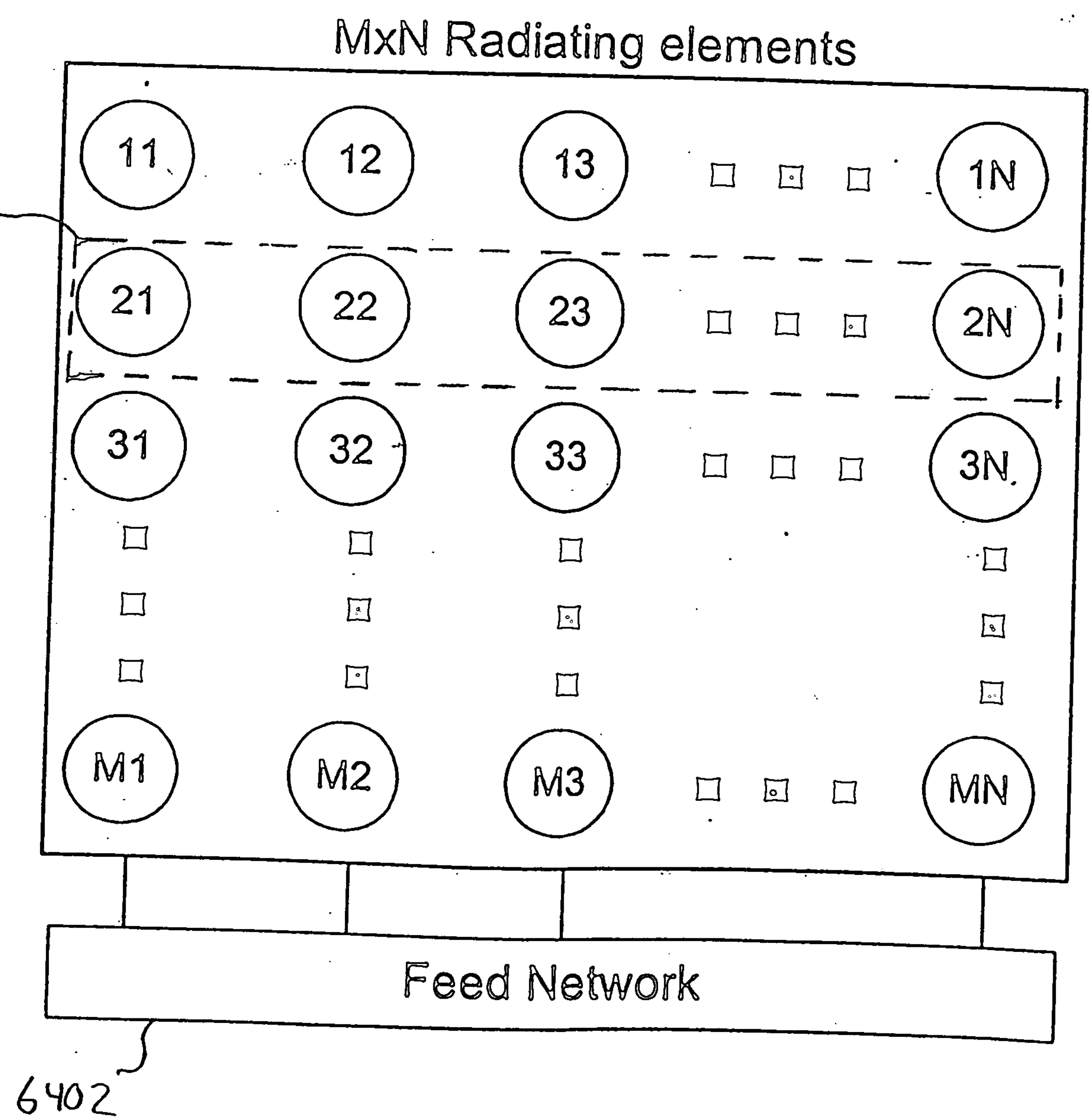


FIG. 63B

6400



MxN Radiating elements
11
12
13
1N
6200
21
22
23
2N
31
32
33
3N
M1
M2
M3
MN
Feed Network
6402

FIG. 64

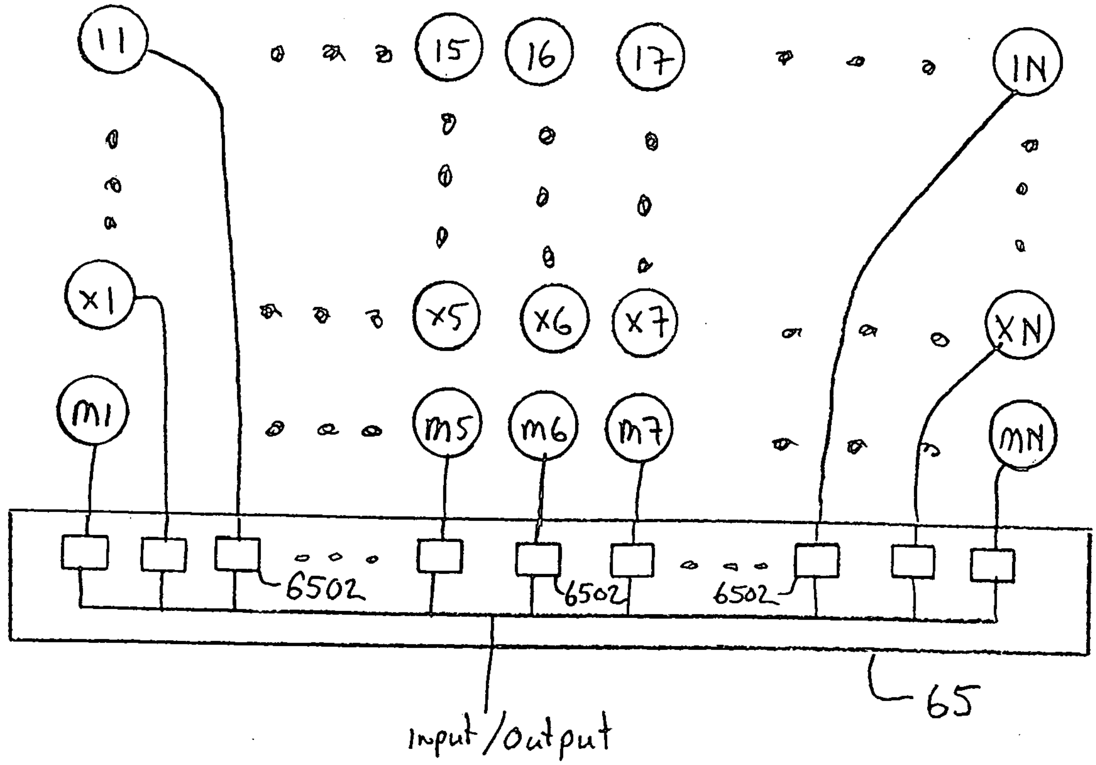


FIG. 65A

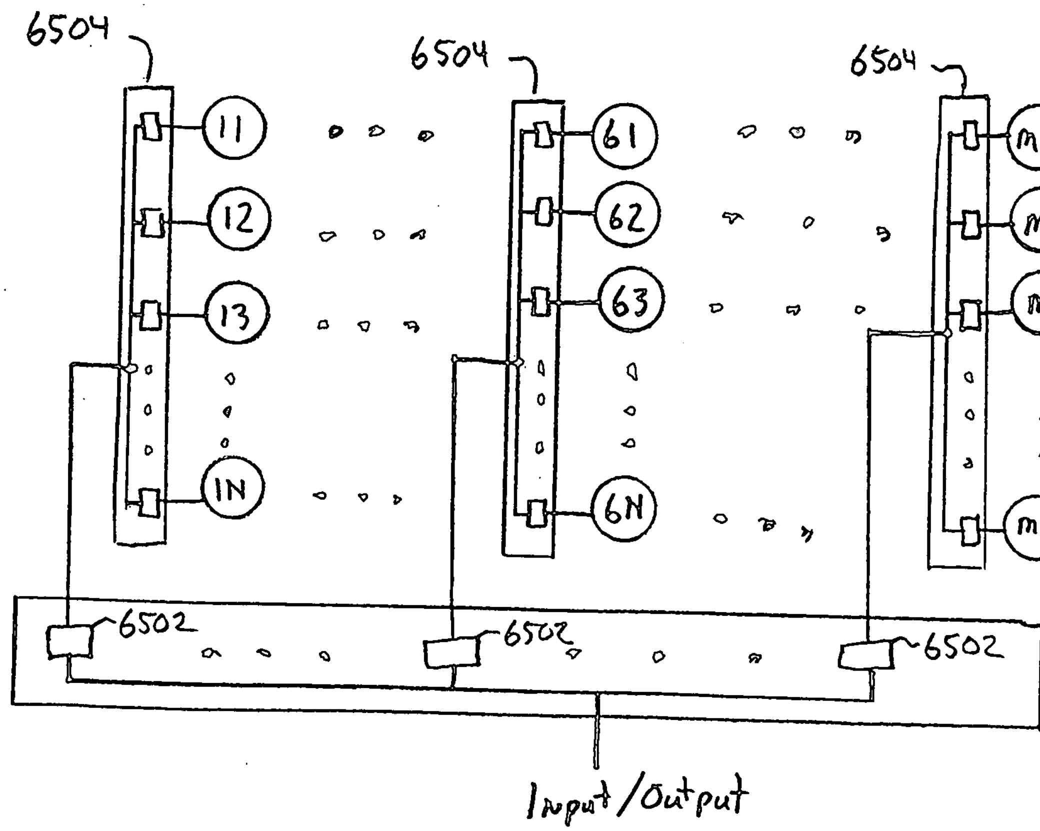


FIG. 65B

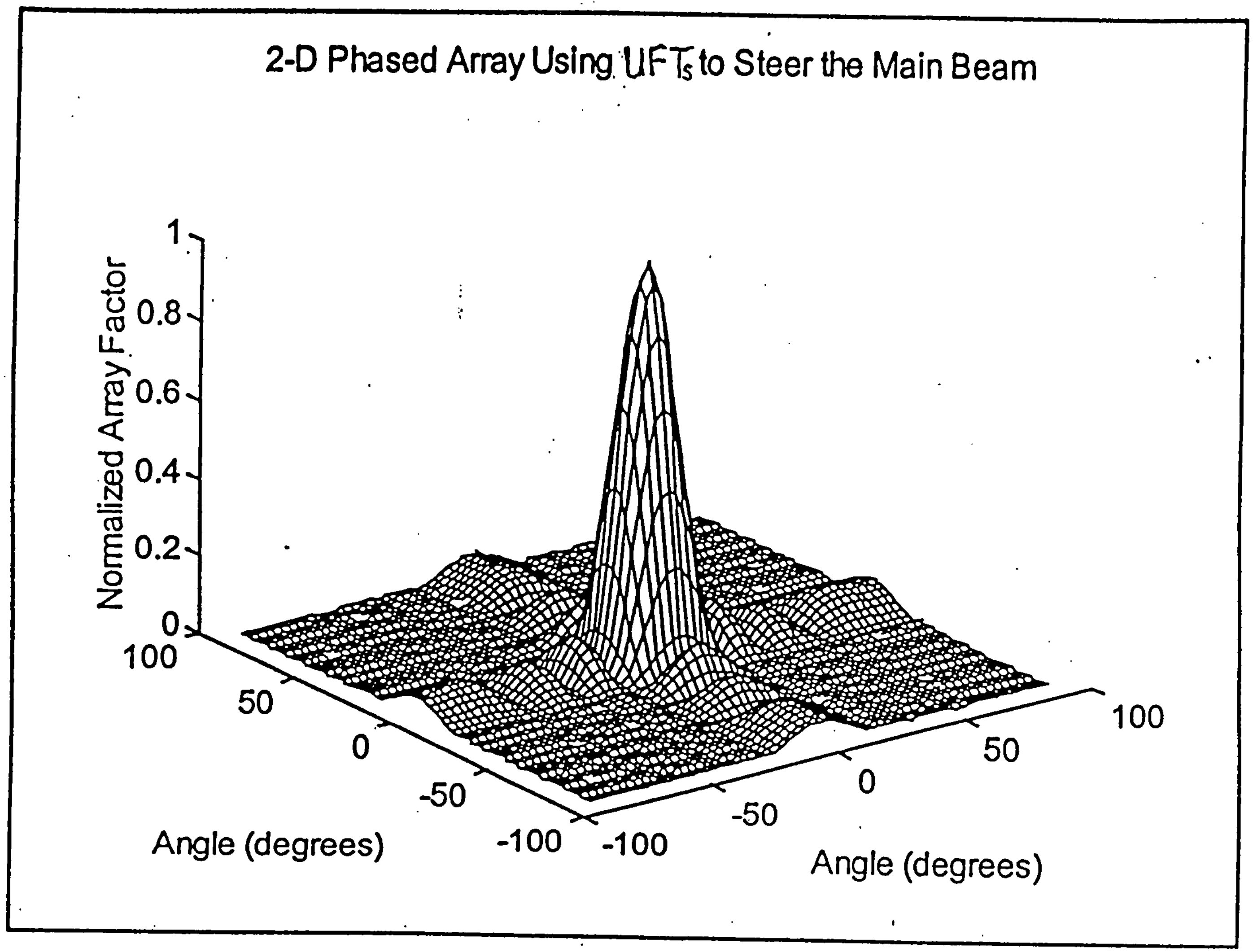

2-D Phased Array Using UFTs to Steer the Main Beam
Normalized Array Factor
1
0.8
0.6
0.4
0.2
0
100
50
0
-50
-100
-100
-50
0
50
100
Angle (degrees)
Angle (degrees)

FIG 66A

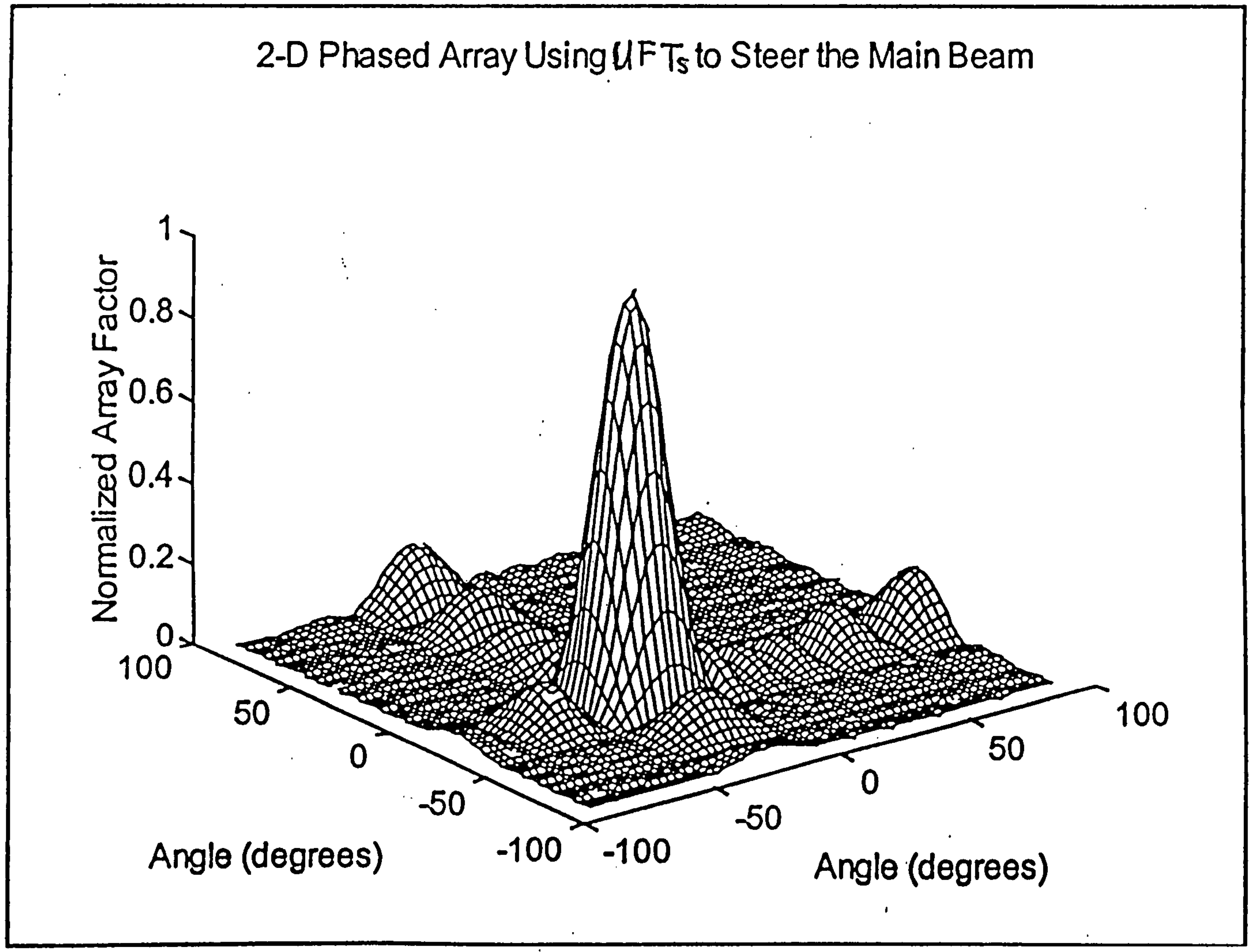

2-D Phased Array Using UFTs to Steer the Main Beam
Normalized Array Factor
1
0.8
0.6
0.4
0.2
0
100
50
0
-50
-100
Angle (degrees)
-100
-50
0
50
100
Angle (degrees)

FIG. 66B

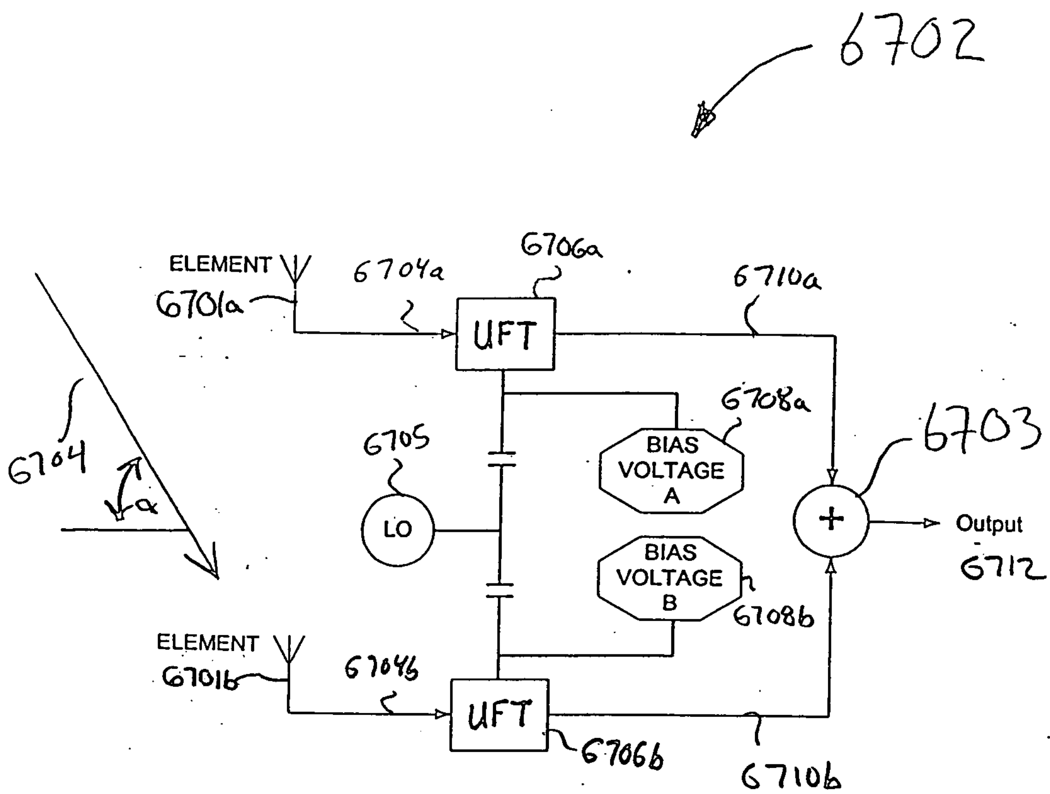


FIG. 67A

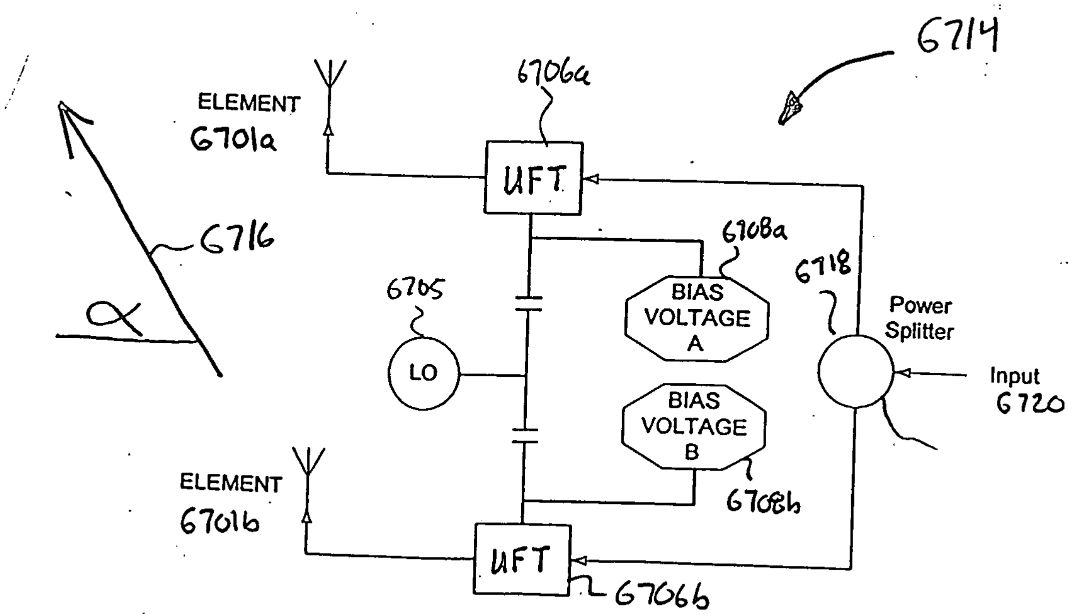
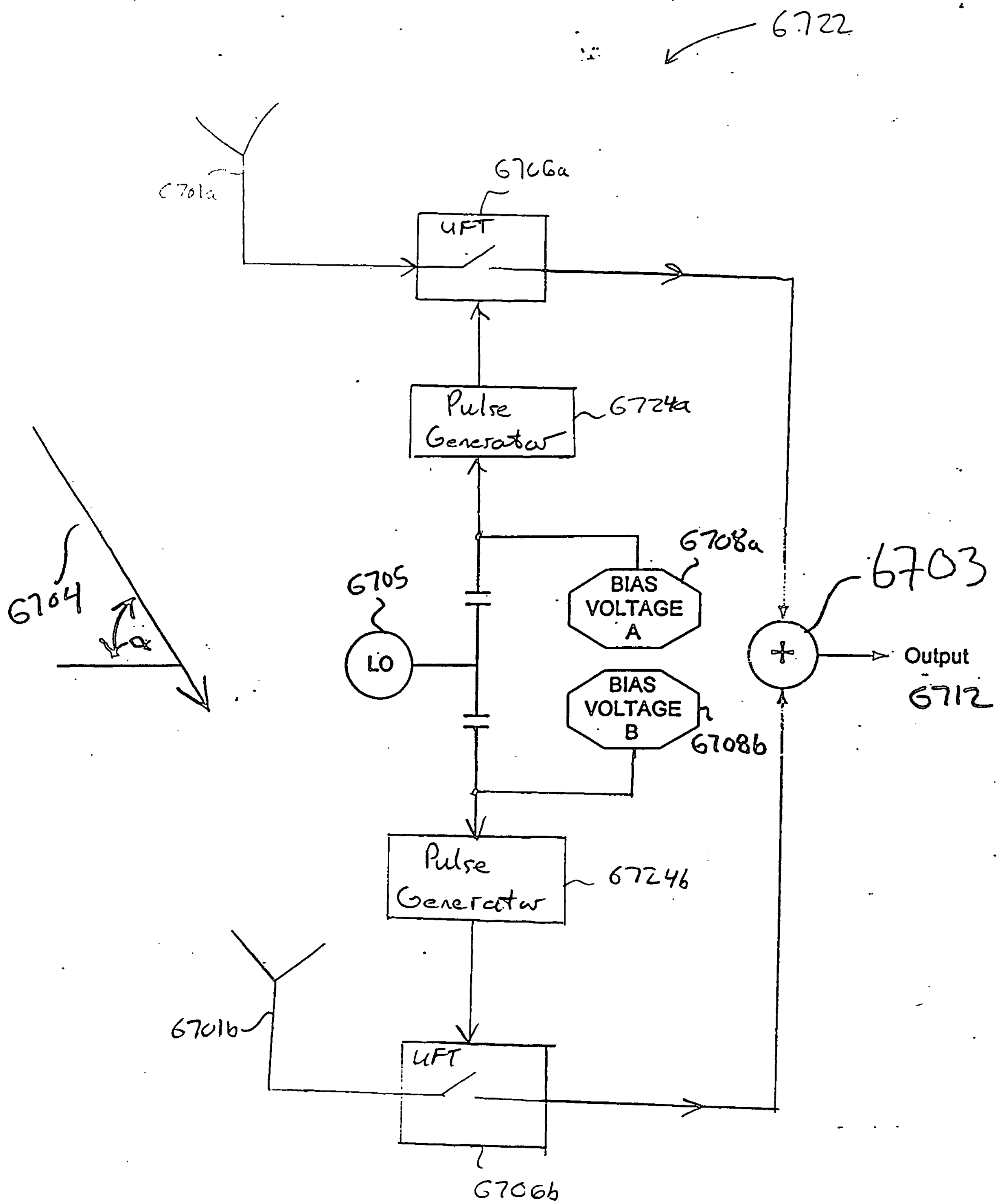


FIG. 67B



6722
6701a
6706a
UFT
Pulse
Generator
6724a
6708a
BIAS
VOLTAGE
A
6705
LO
6704
α
BIAS
VOLTAGE
B
6708b
6703
+
Output
6712
Pulse
Generator
6724b
6701b
UFT
6706b

FIG. 67C

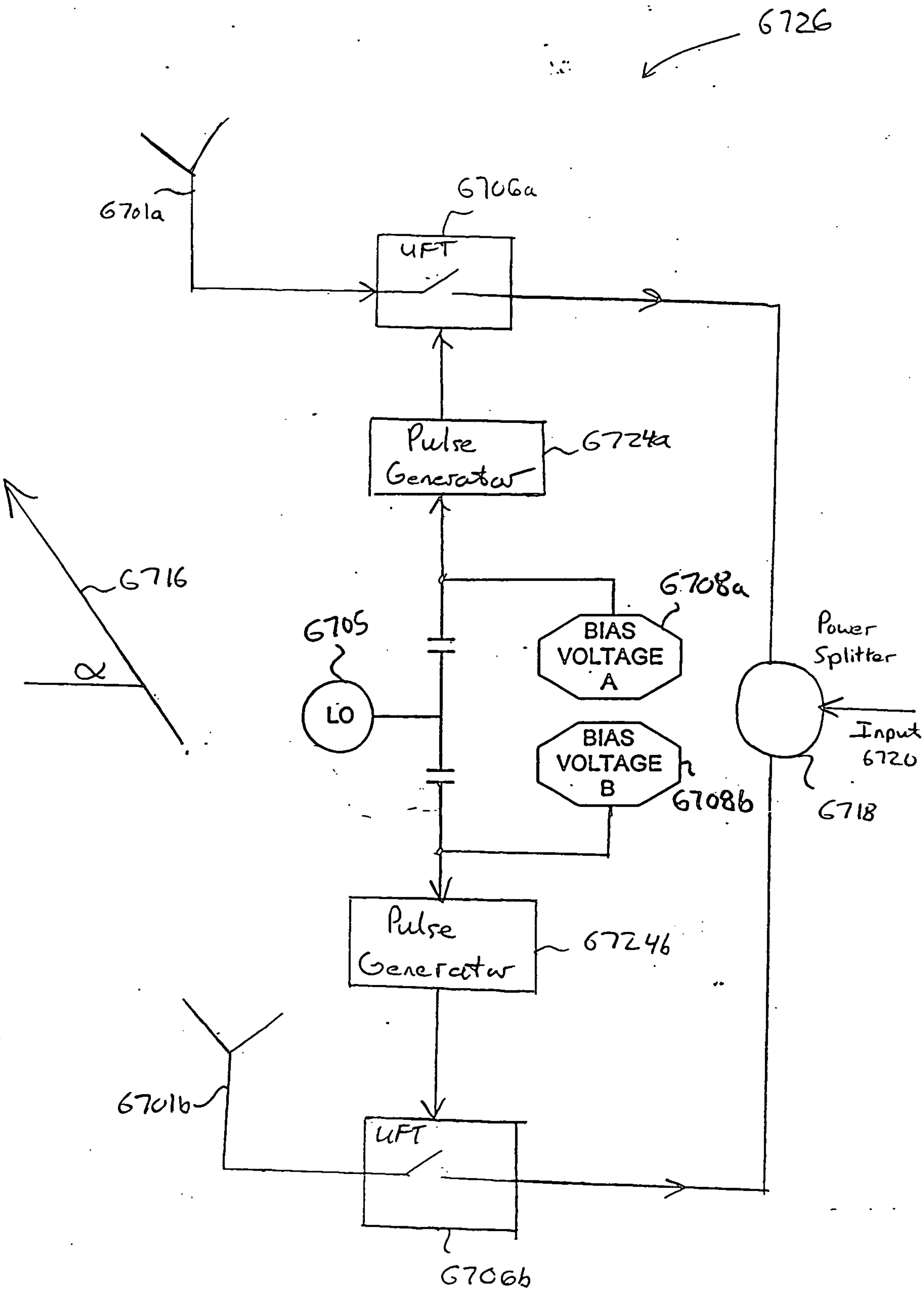

6726
6701a
6706a
UFT
Pulse Generator
6724a
6716
α
6708a
BIAS VOLTAGE A
6705
LO
BIAS VOLTAGE B
6708b
Power Splitter
Input 6720
6718
Pulse Generator
6724b
6701b
UFT
6706b

FIG. 67D

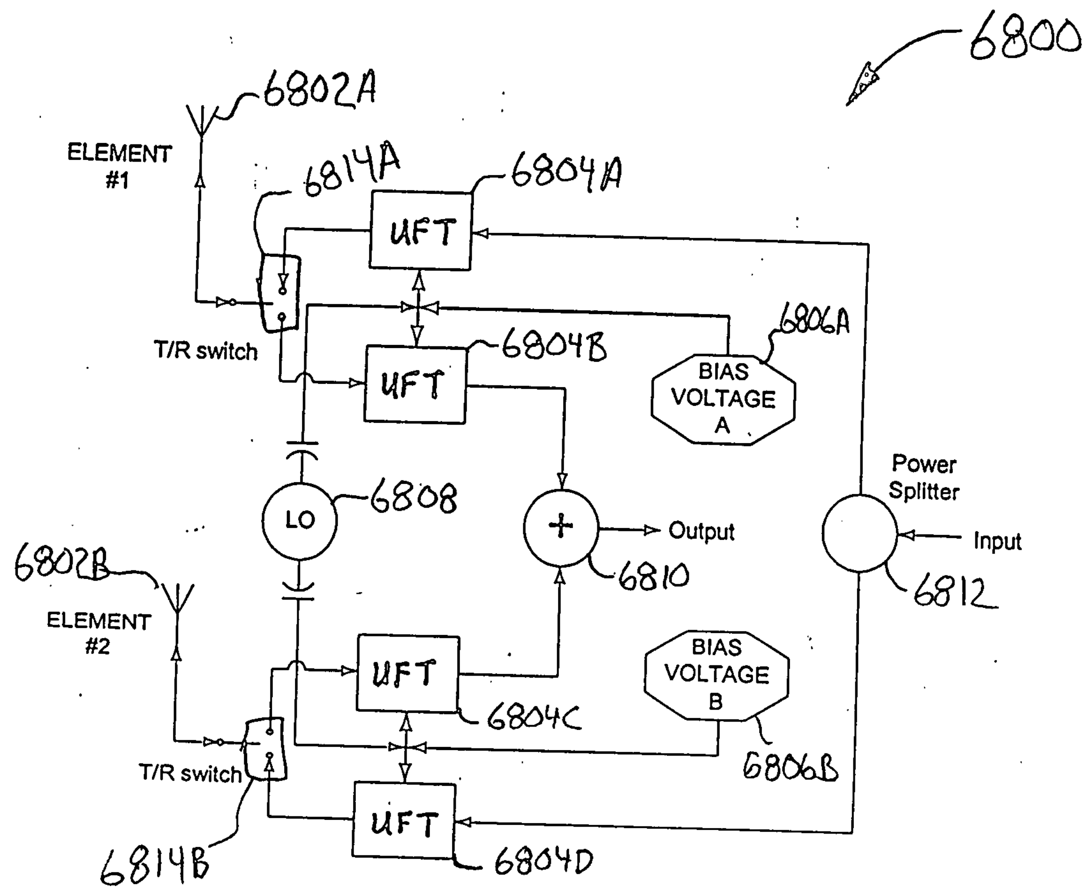

6800
6802A
ELEMENT #1
6814A
6804A
UFT
T/R switch
6804B
UFT
6806A
BIAS VOLTAGE A
Power Splitter
LO
6808
+
Output
Input
6810
6812
6802B
ELEMENT #2
UFT
BIAS VOLTAGE B
6804C
T/R switch
6806B
UFT
6814B
6804D

FIG. 68A

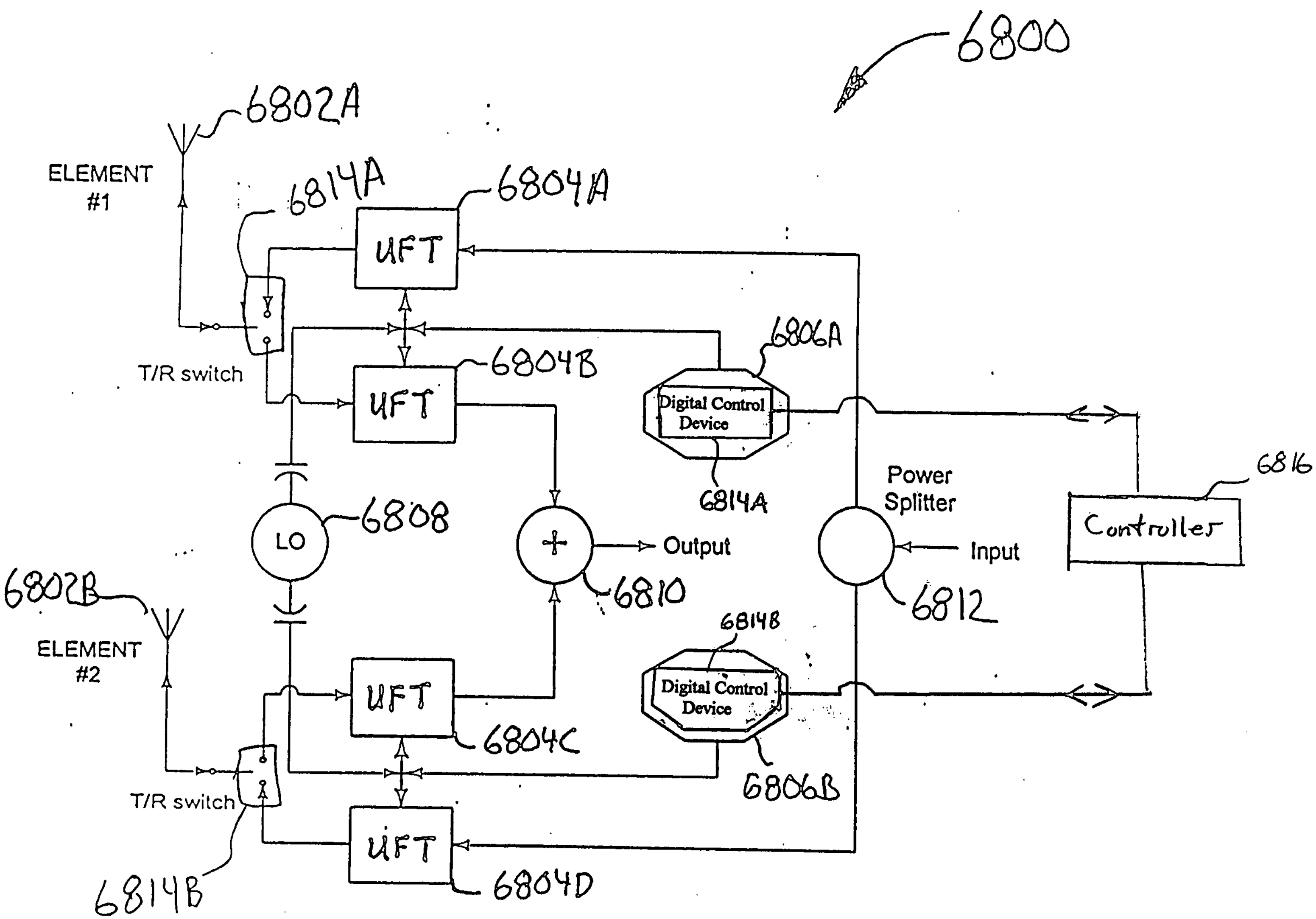

6800
6802A
ELEMENT #1
6814A
6804A
UFT
T/R switch
6804B
UFT
6806A
Digital Control Device
6814A
LO
6808
Output
6810
Power Splitter
Input
6812
6816
Controller
6802B
ELEMENT #2
6814B
Digital Control Device
UFT
6804C
6806B
T/R switch
UFT
6814B
6804D

FIG. 68B

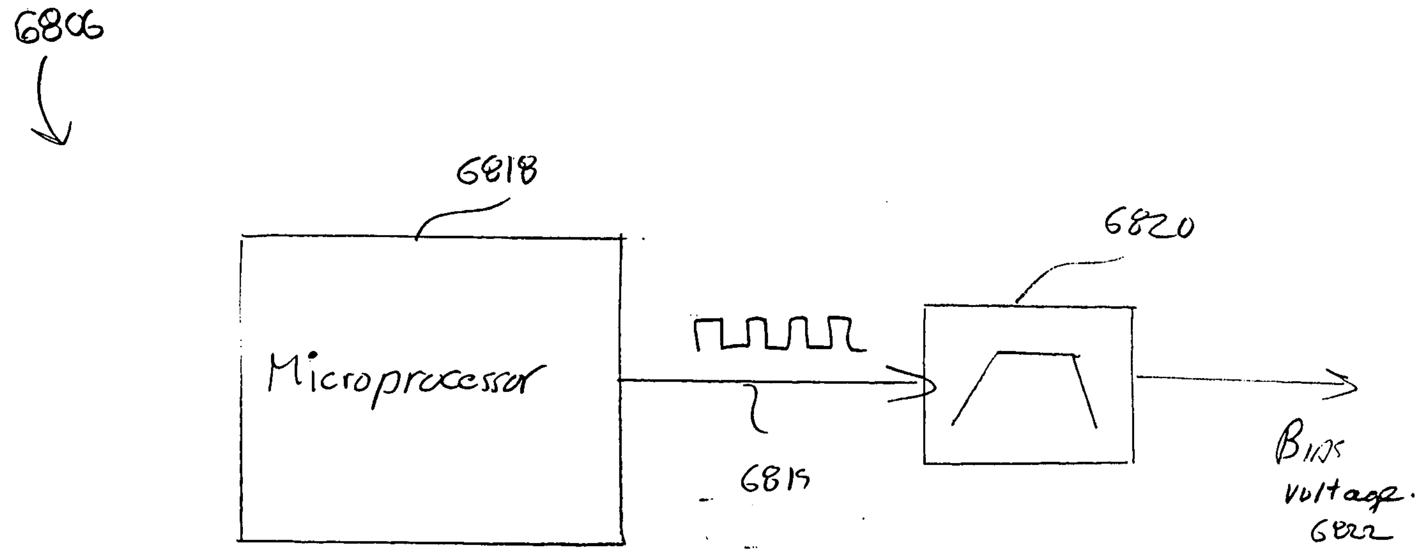


FIG. 68C

Radiation Pattern for a UFT Based, Two Element Phased Array
15 Degree Main Beam Angle, -20 Degree Null

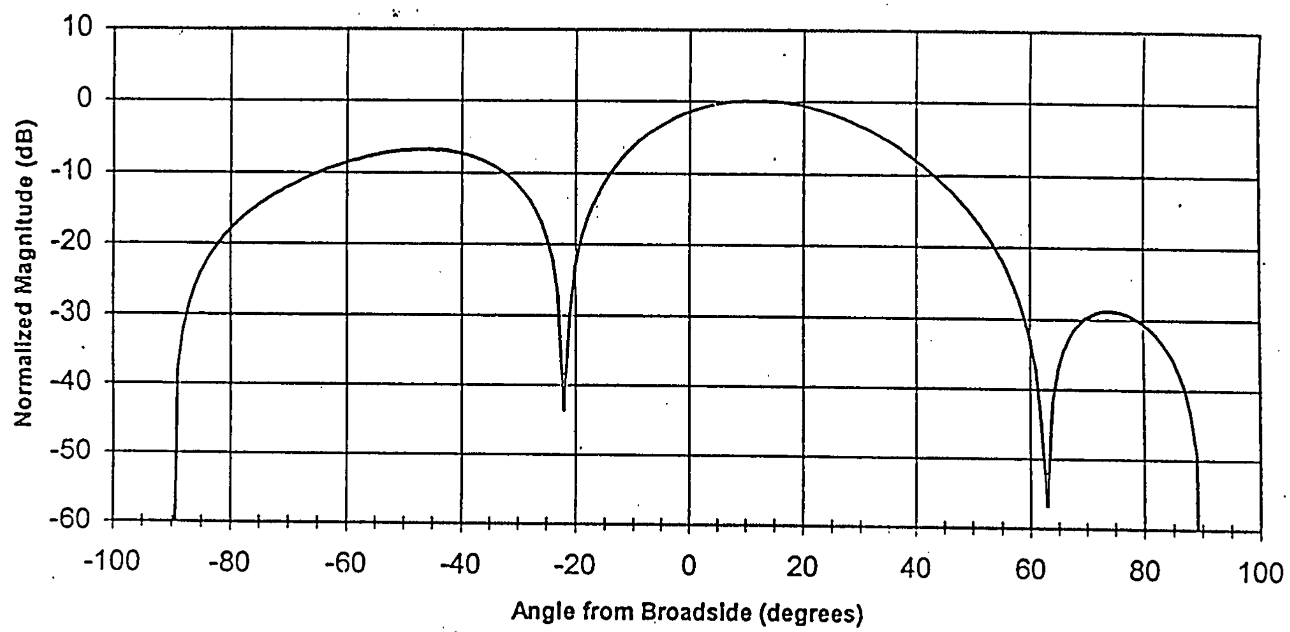


FIG. 69

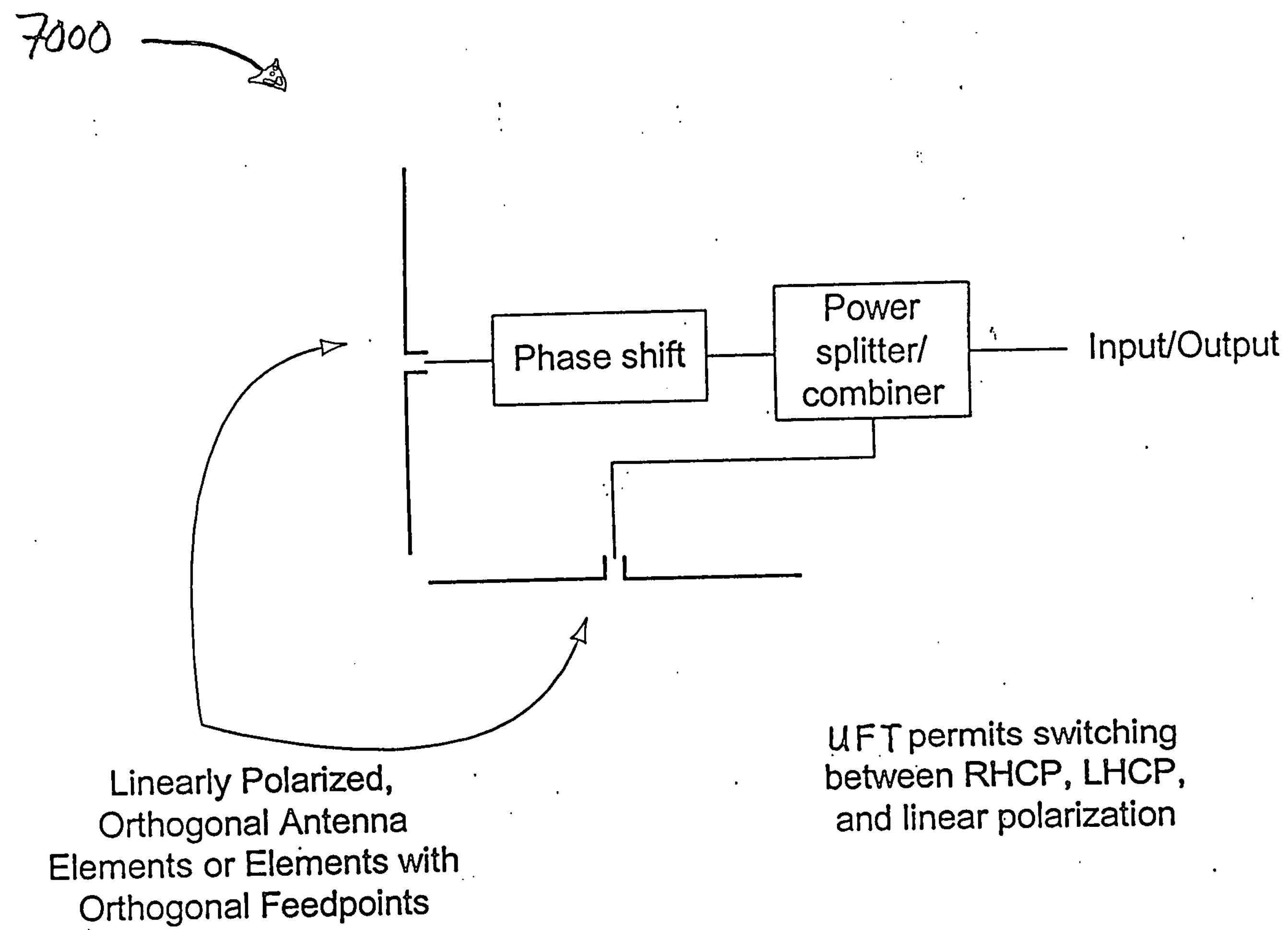

7000
Phase shift
Power splitter/ combiner
Input/Output
Linearly Polarized, Orthogonal Antenna Elements or Elements with Orthogonal Feedpoints
UFT permits switching between RHCP, LHCP, and linear polarization

FIG. 70

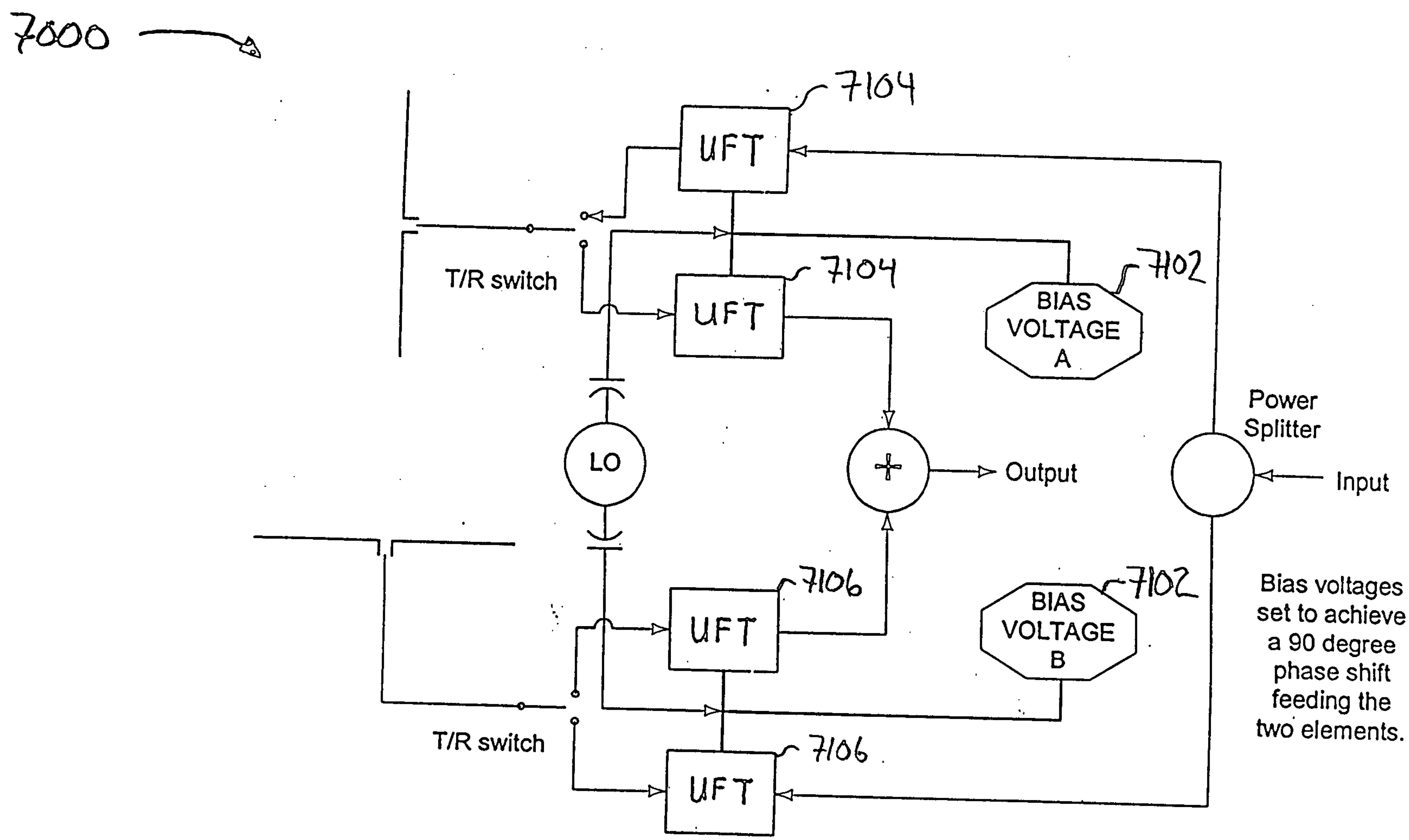
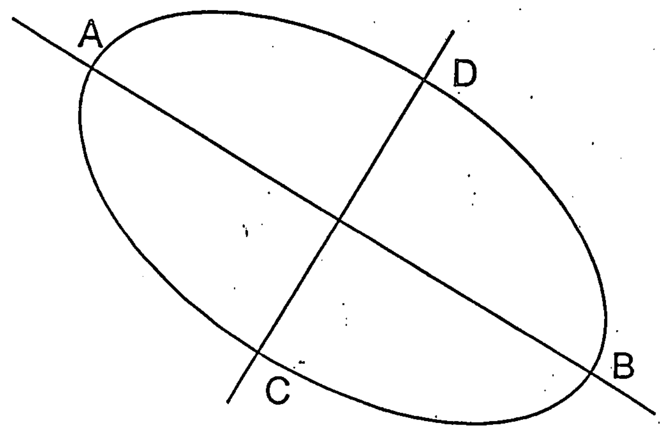

7000
7104
UFT
7104
UFT
7102
BIAS
VOLTAGE
A
T/R switch
LO
+
Output
Power
Splitter
Input
7106
UFT
7102
BIAS
VOLTAGE
B
T/R switch
7106
UFT
Bias voltages
set to achieve
a 90 degree
phase shift
feeding the
two elements.

FIG. 71



Ellipse representing an
elliptically polarized wave

The axial ratio is the ratio of the length of the line segment AB to the length of the line segment CD

$$\text{Axial Ratio} = \frac{AB}{CD}$$

When AB=CD then the ideal axial ratio is achieved and pure circular polarization is realized

FIG. 72

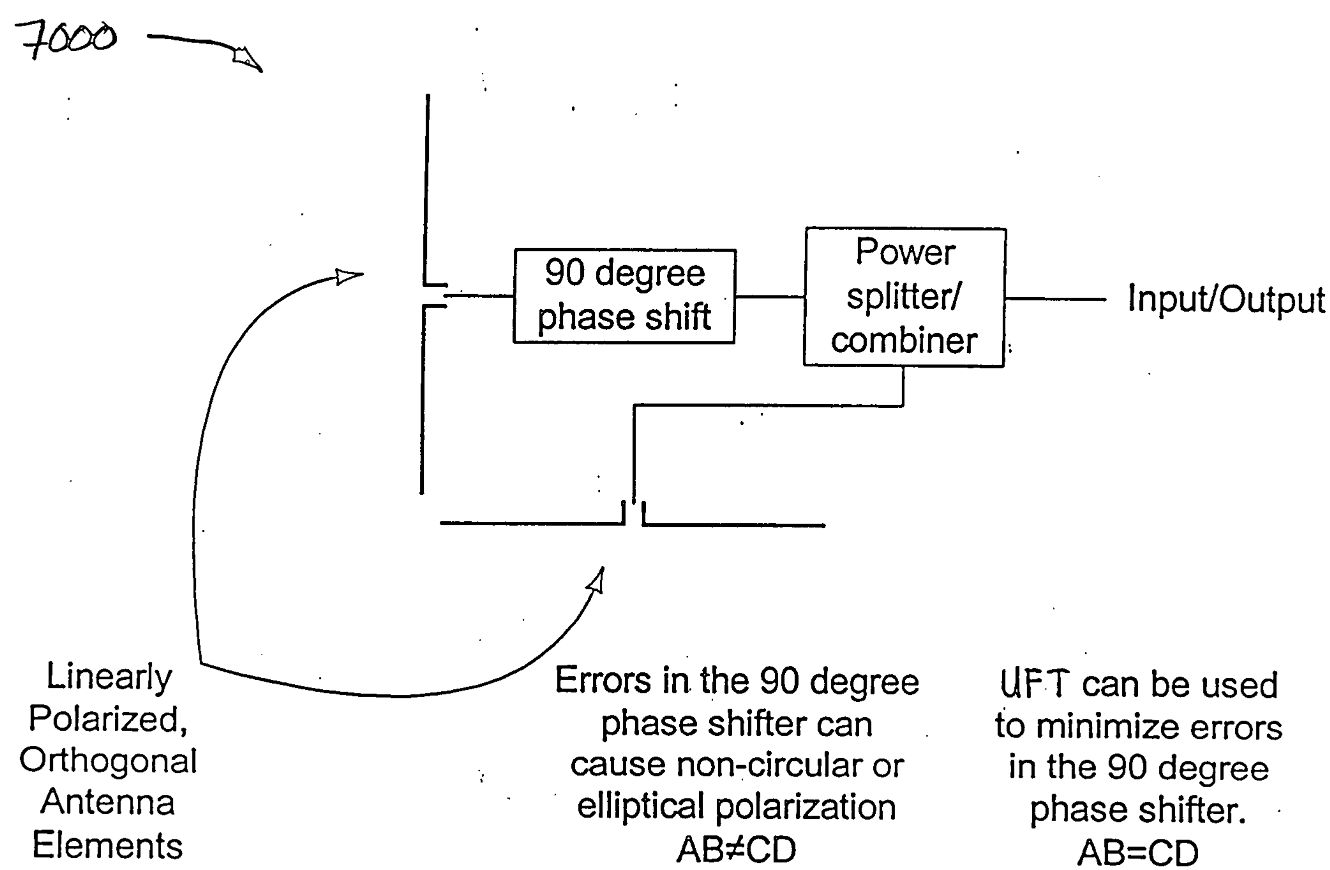

7000
90 degree phase shift
Power splitter/ combiner
Input/Output
Linearly Polarized, Orthogonal Antenna Elements
Errors in the 90 degree phase shifter can cause non-circular or elliptical polarization AB≠CD
UFT can be used to minimize errors in the 90 degree phase shifter. AB=CD

FIG. 73

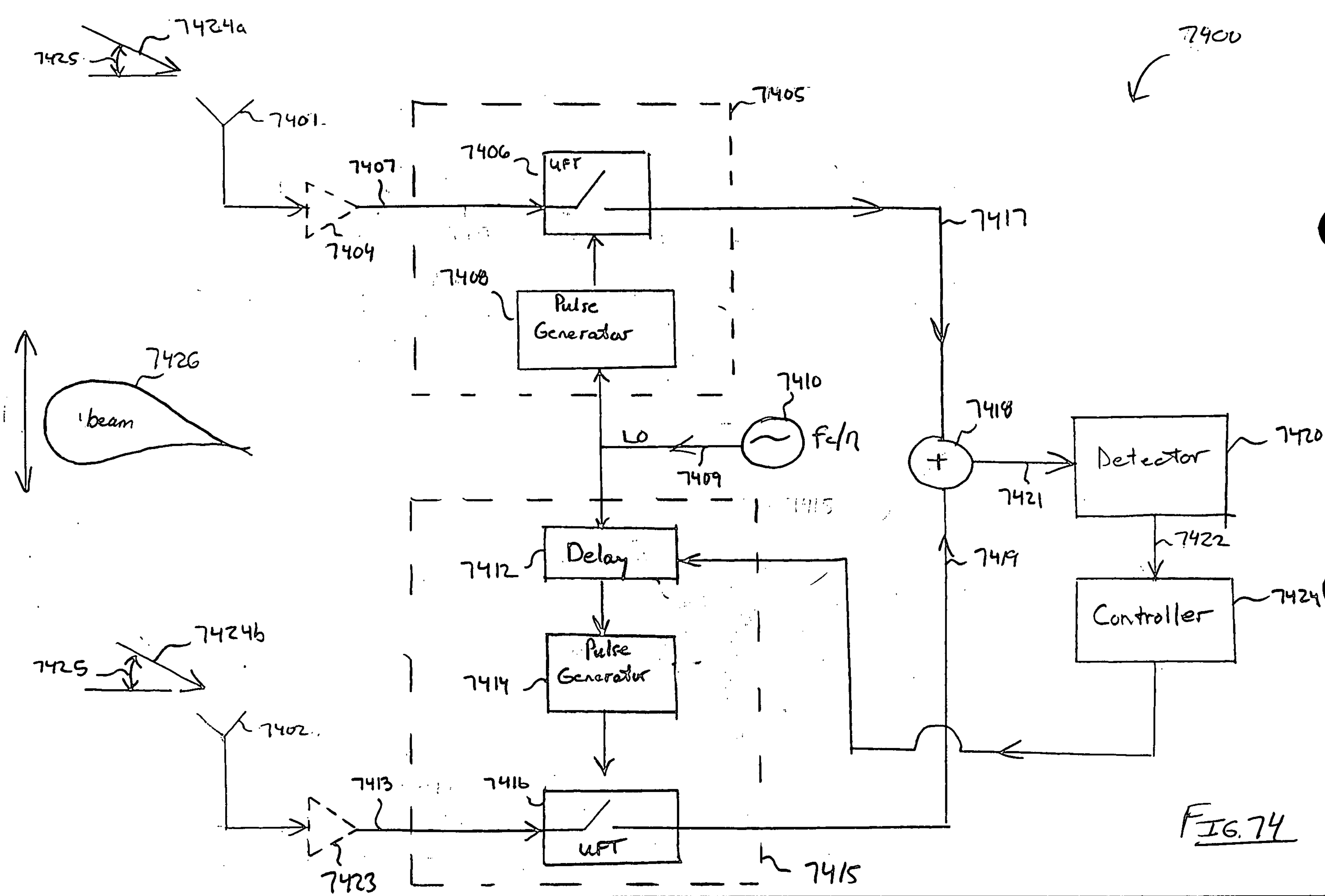

7400
7424a
7425
7401
7407
7404
7405
7406
UFT
7408
Pulse Generator
7417
7426
beam
7410
fc/n
LO
7409
7418
+
7421
Detector
7420
7422
Controller
7424
7419
Delay
7412
7424b
7425
Pulse Generator
7414
7402
7413
7416
UFT
7423
7415

FIG. 74

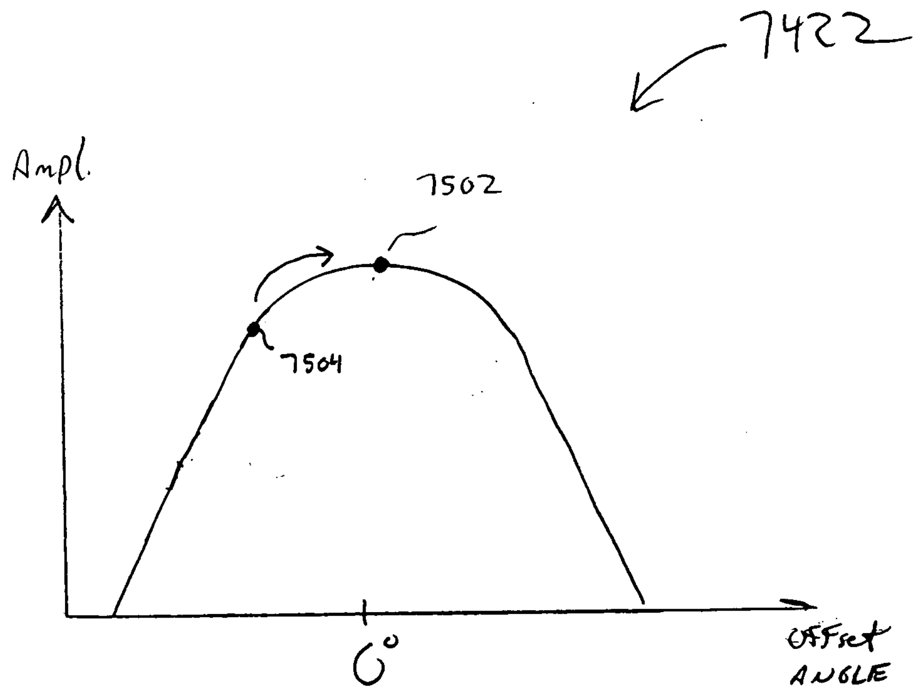


FIG. 75

006090"SS606S60

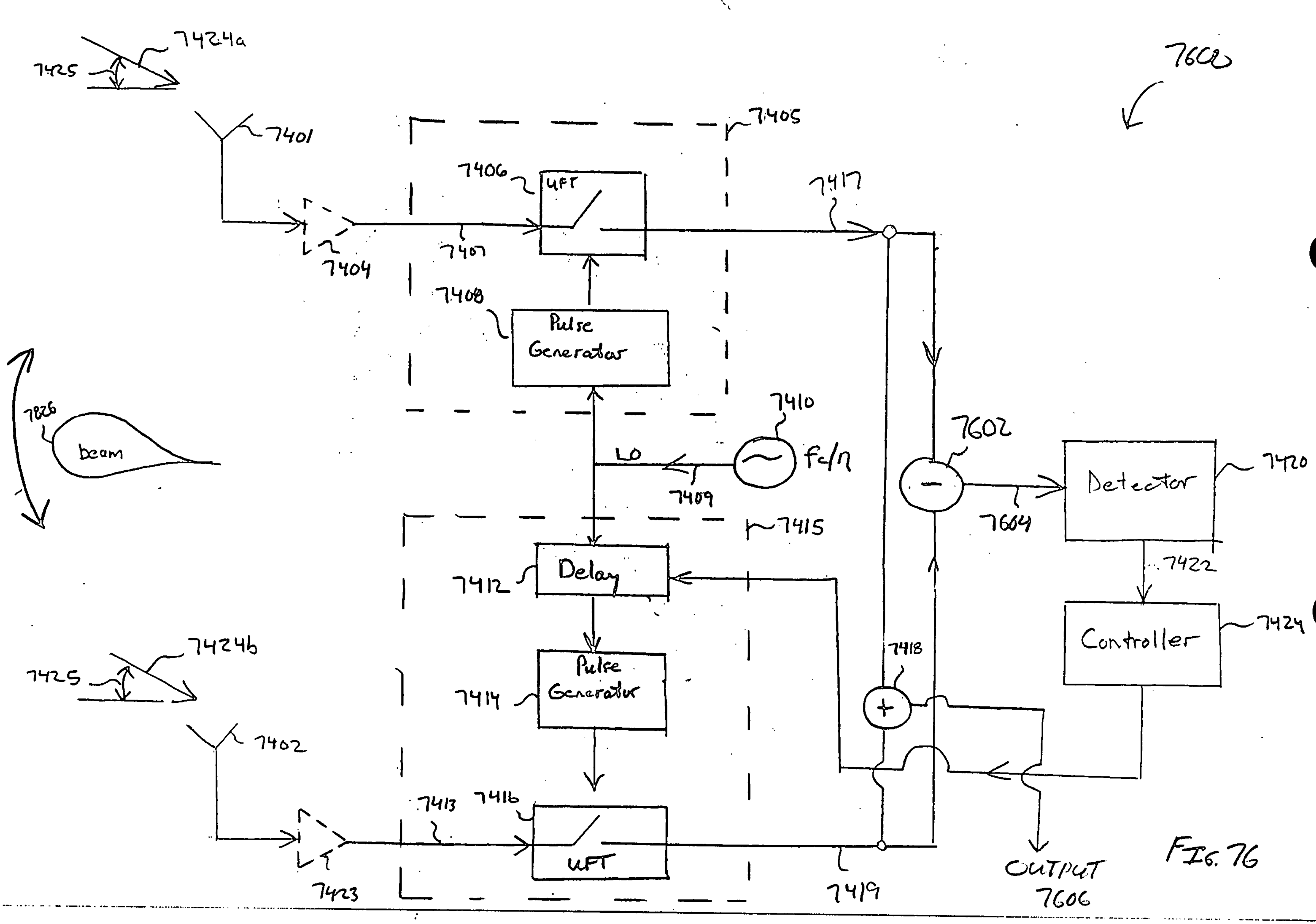


FIG. 76

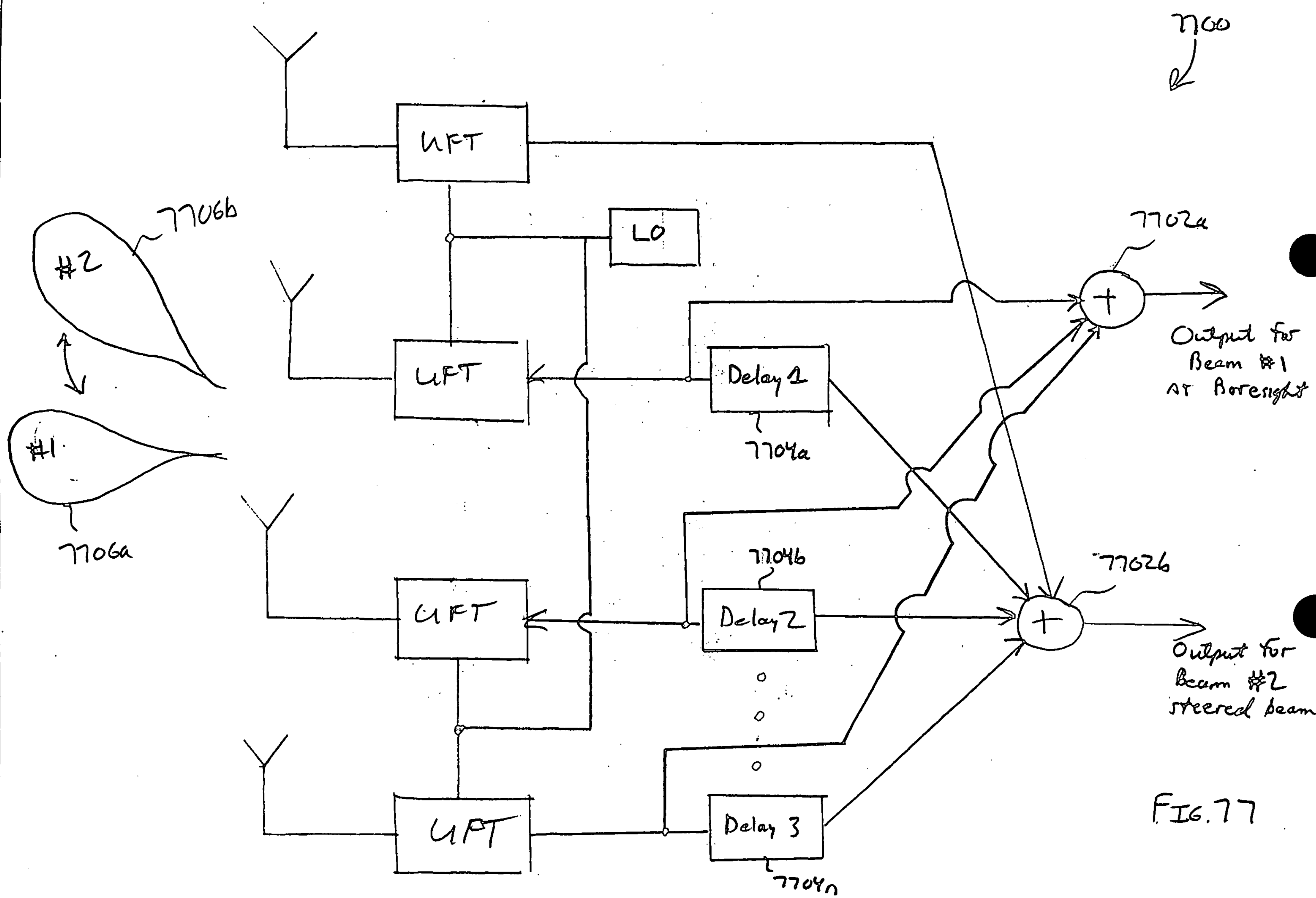

7700
UFT
UFT
UFT
UFT
LO
Delay 1
Delay 2
Delay 3
7704a
7704b
7704n
7702a
7702b
7706a
7706b
#1
#2
Output for Beam #1 at Boresight
Output for Beam #2 steered beam

FIG. 77

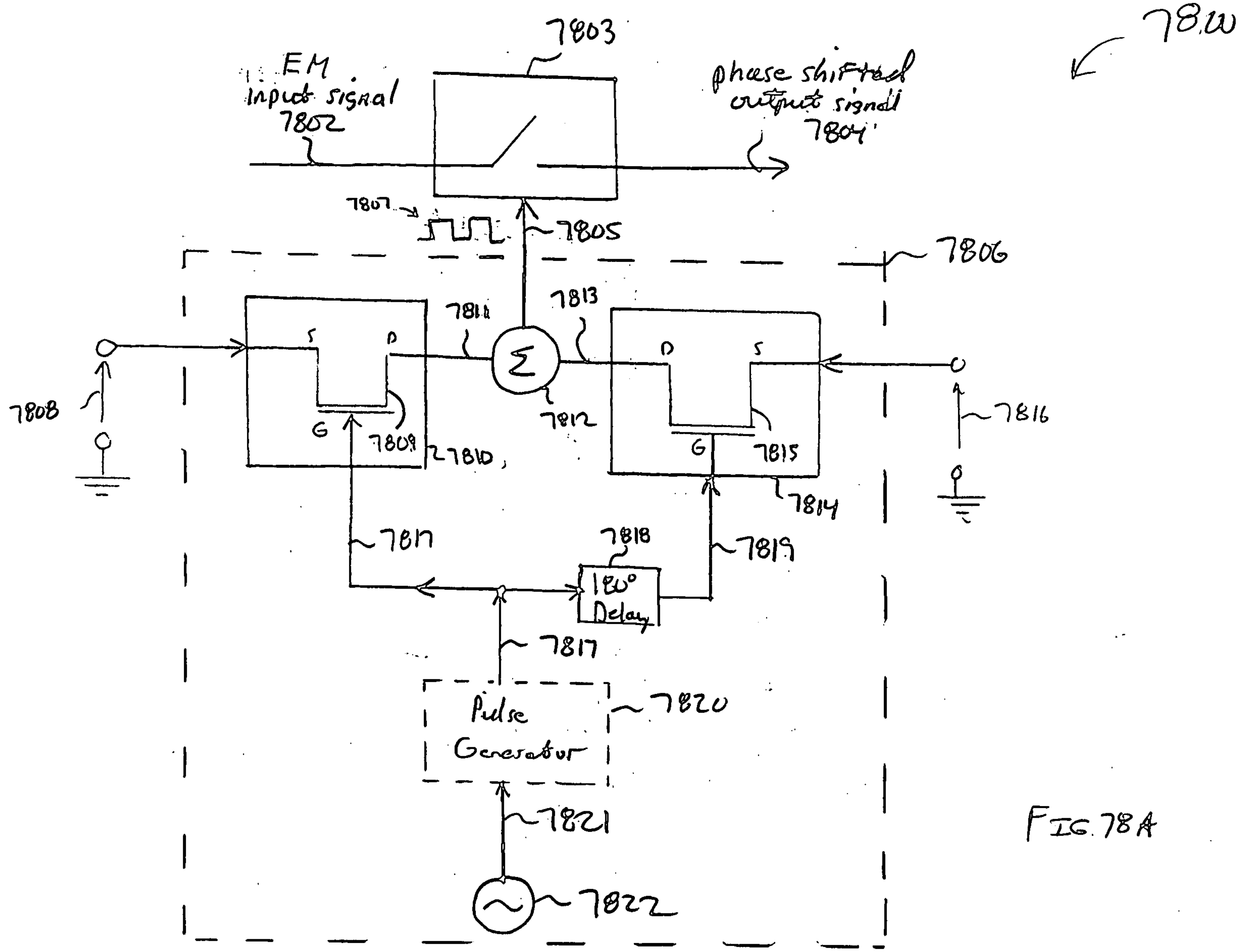

78W
EM
input signal
7802
7803
phase shifted
output signal
7804'
7807
7805
7806
S
D
G
7809
7810
7811
7812
7813
D
S
G
7815
7814
7808
7816
7817
7818
180°
Delay
7819
7817
Pulse
Generator
7820
7821
7822

FIG. 78A

FIG. 78B

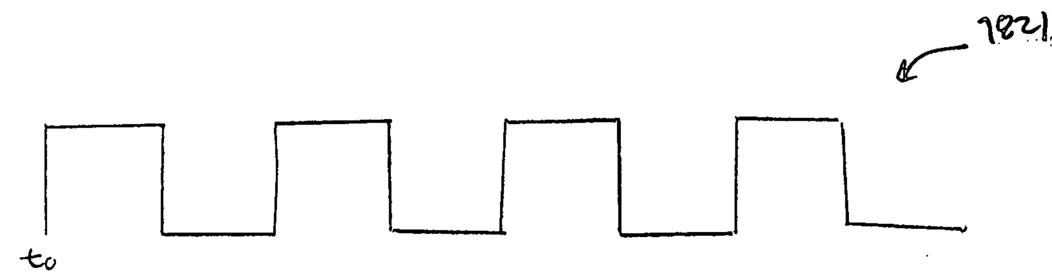
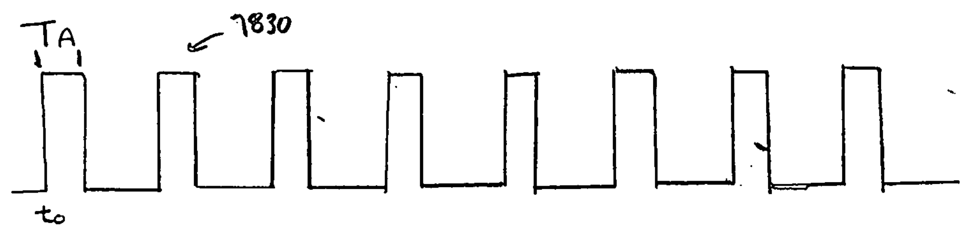


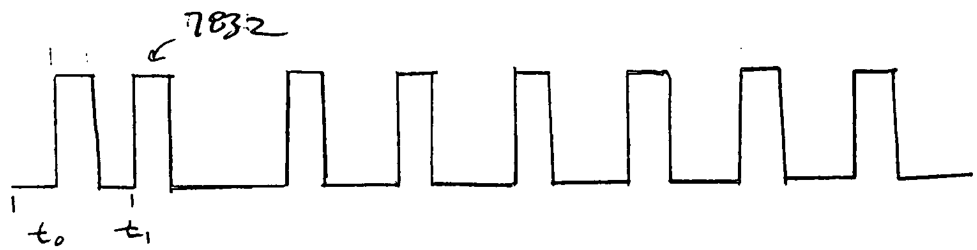
FIG. 78C



7805

for DC 7808 = DC 7816

FIG. 78D



7805

for DC 7808 ≠ DC 7816 AT T_1

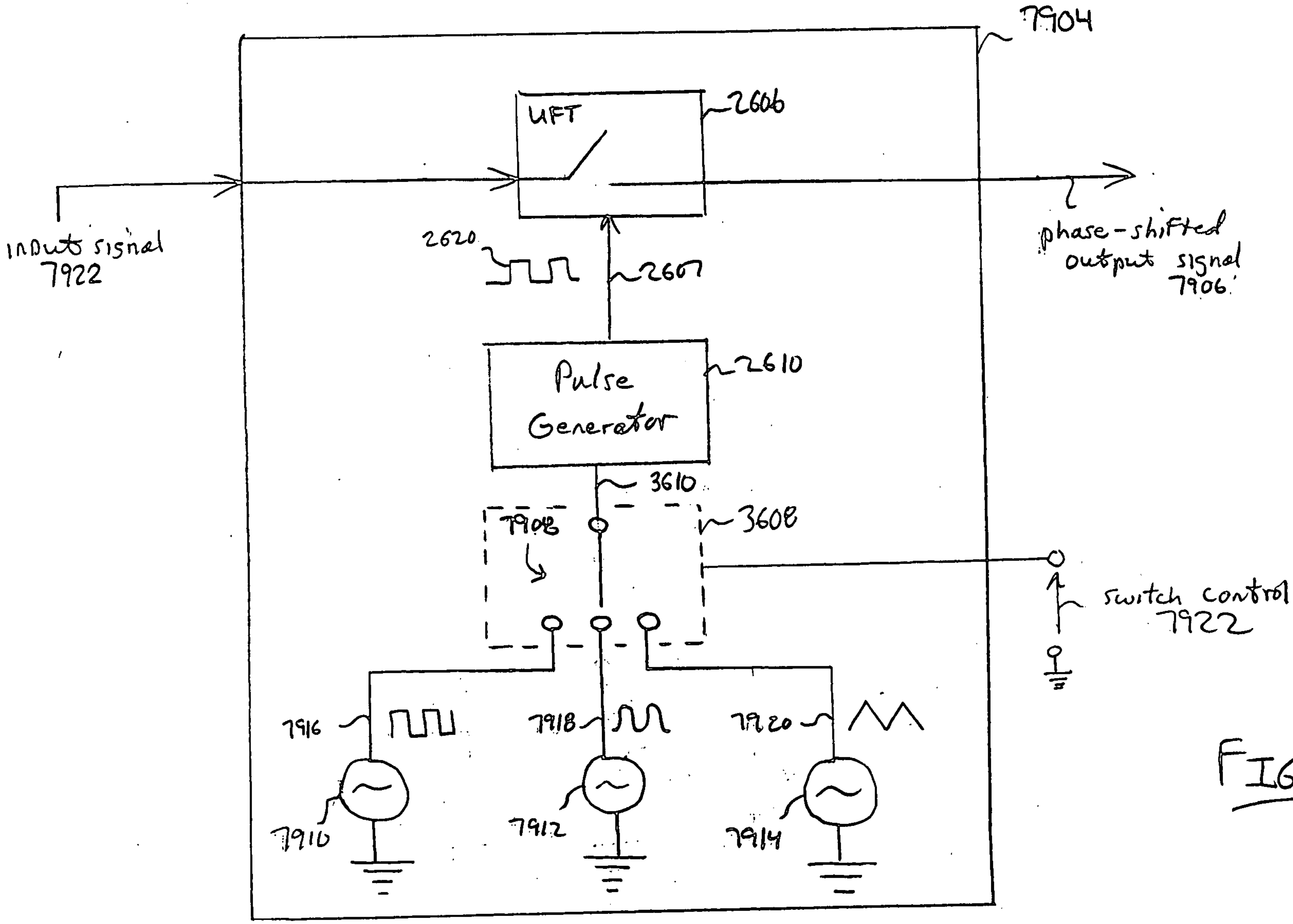

7904
UFT
2606
input signal
7922
phase-shifted
output signal
7906
2620
2607
Pulse
Generator
2610
3610
7908
3608
switch control
7922
7916
7918
7920
7910
7912
7914

FIG. 79

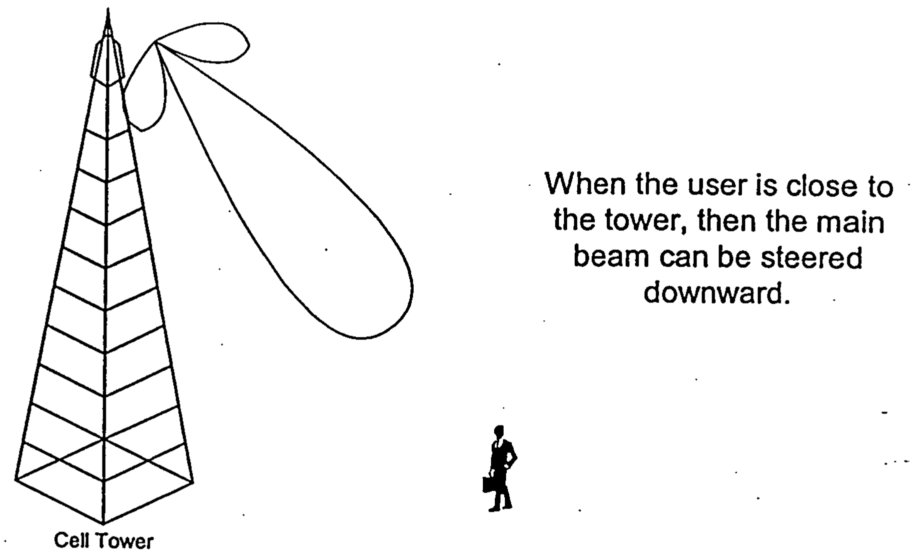


FIG. 80A

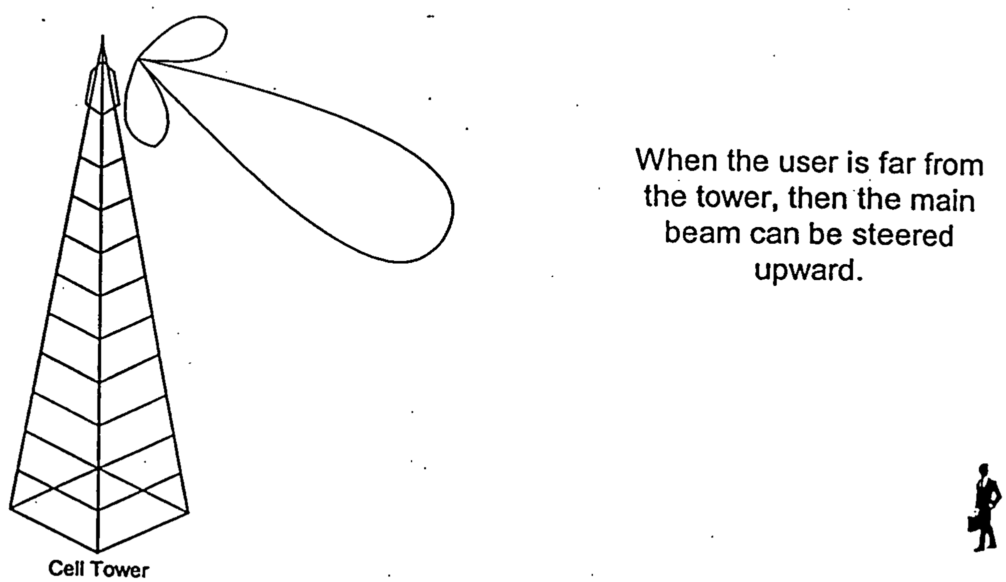


FIG. 80B

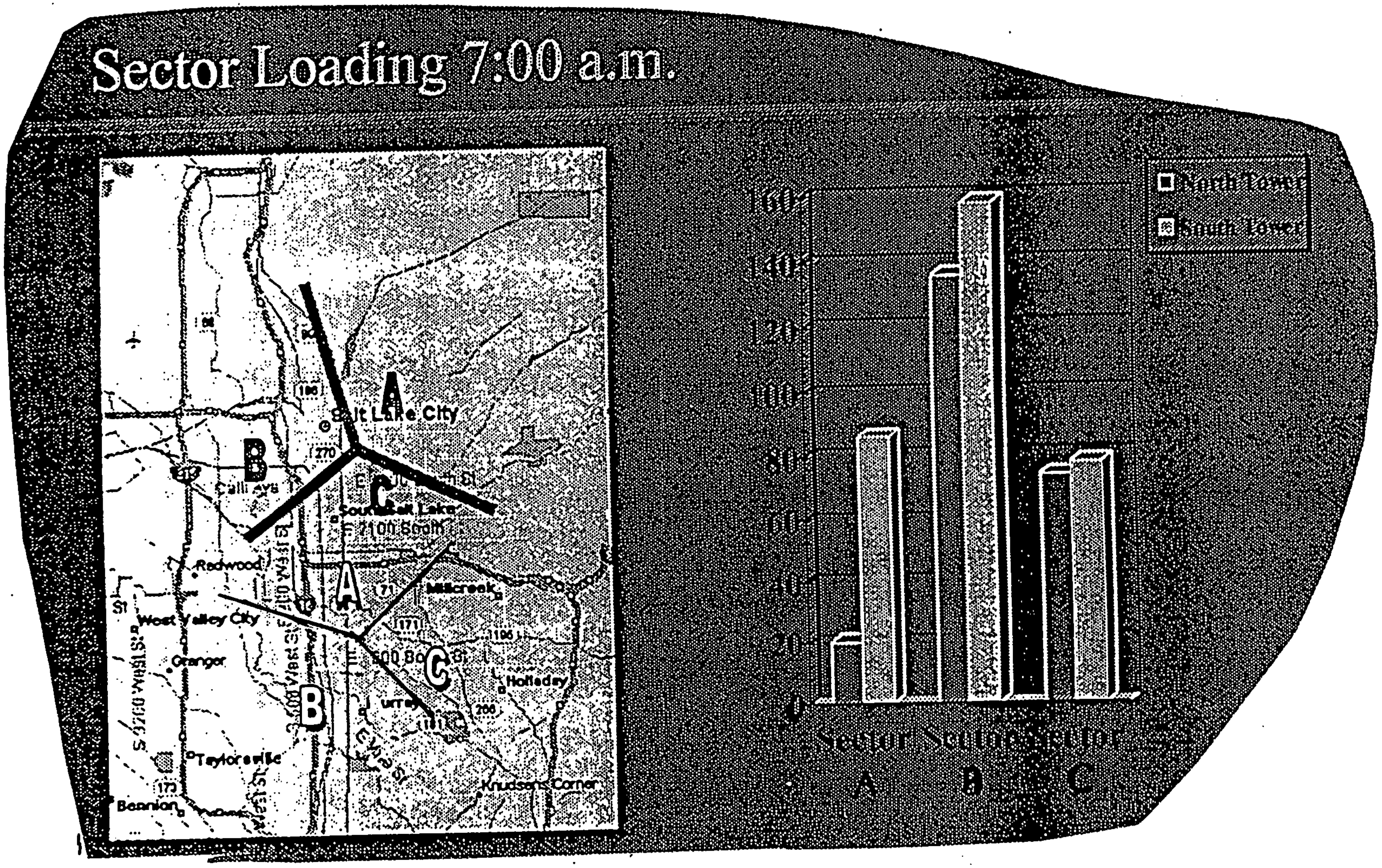

Sector Loading 7:00 a.m.
Salt Lake City
South Salt Lake
Redwood
West Valley City
Millcreek
Holladay
Granger
Taylorsville
Bennion
Knudsens Corner
A
B
C
North Tower
South Tower
0
20
40
60
80
100
120
140
160
Sector A
Sector B
Sector C

FIG. 81

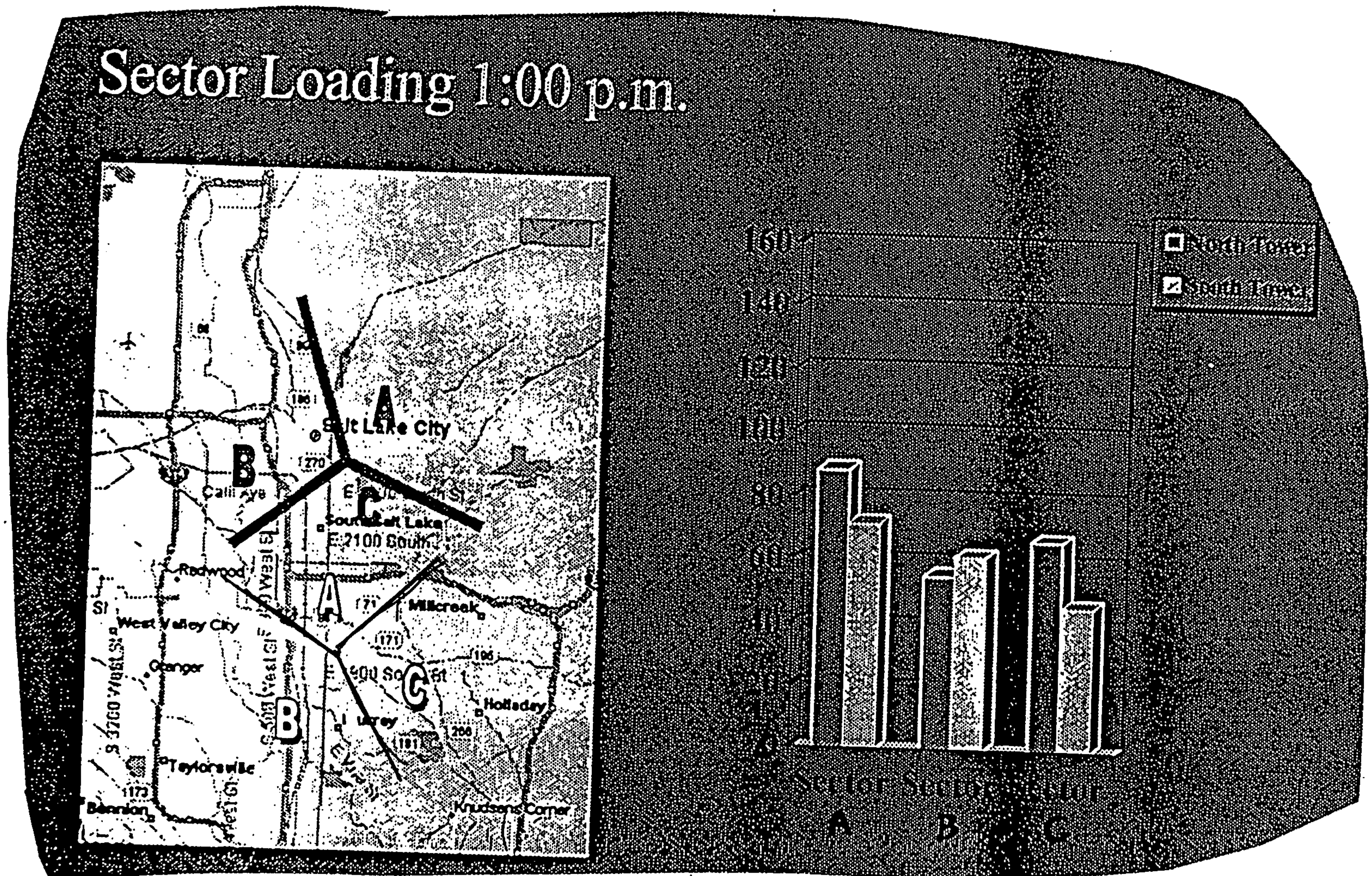

Sector Loading 1:00 p.m.
Salt Lake City
Redwood
West Valley City
Millcreek
Holladay
Taylorsville
Bennion
Knudsens Corner
E 2100 South
A
B
C
A
B
C
160
140
120
100
80
60
40
20
0
North Tower
South Tower
Sector A
Sector B
Sector C

FIG. 82

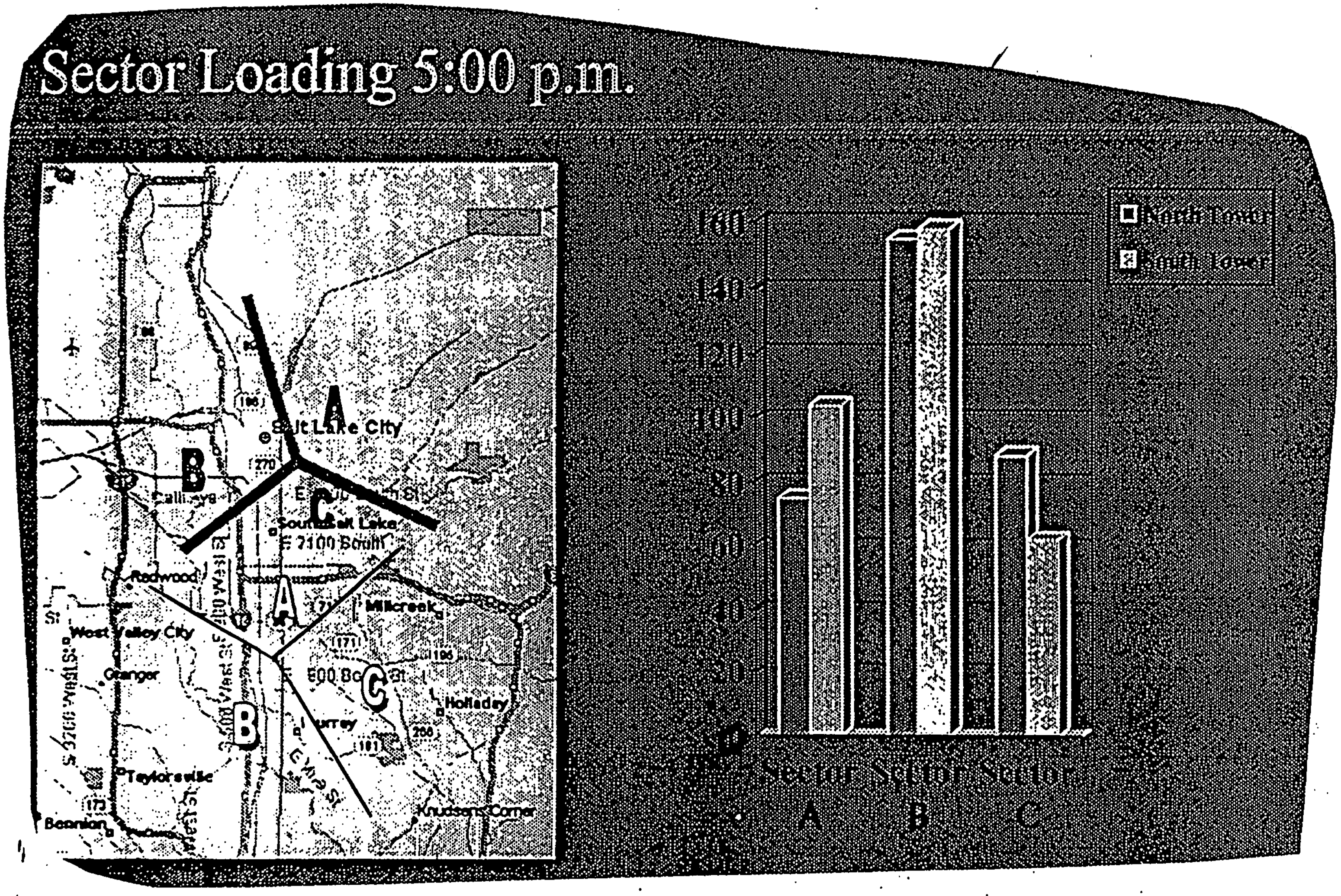
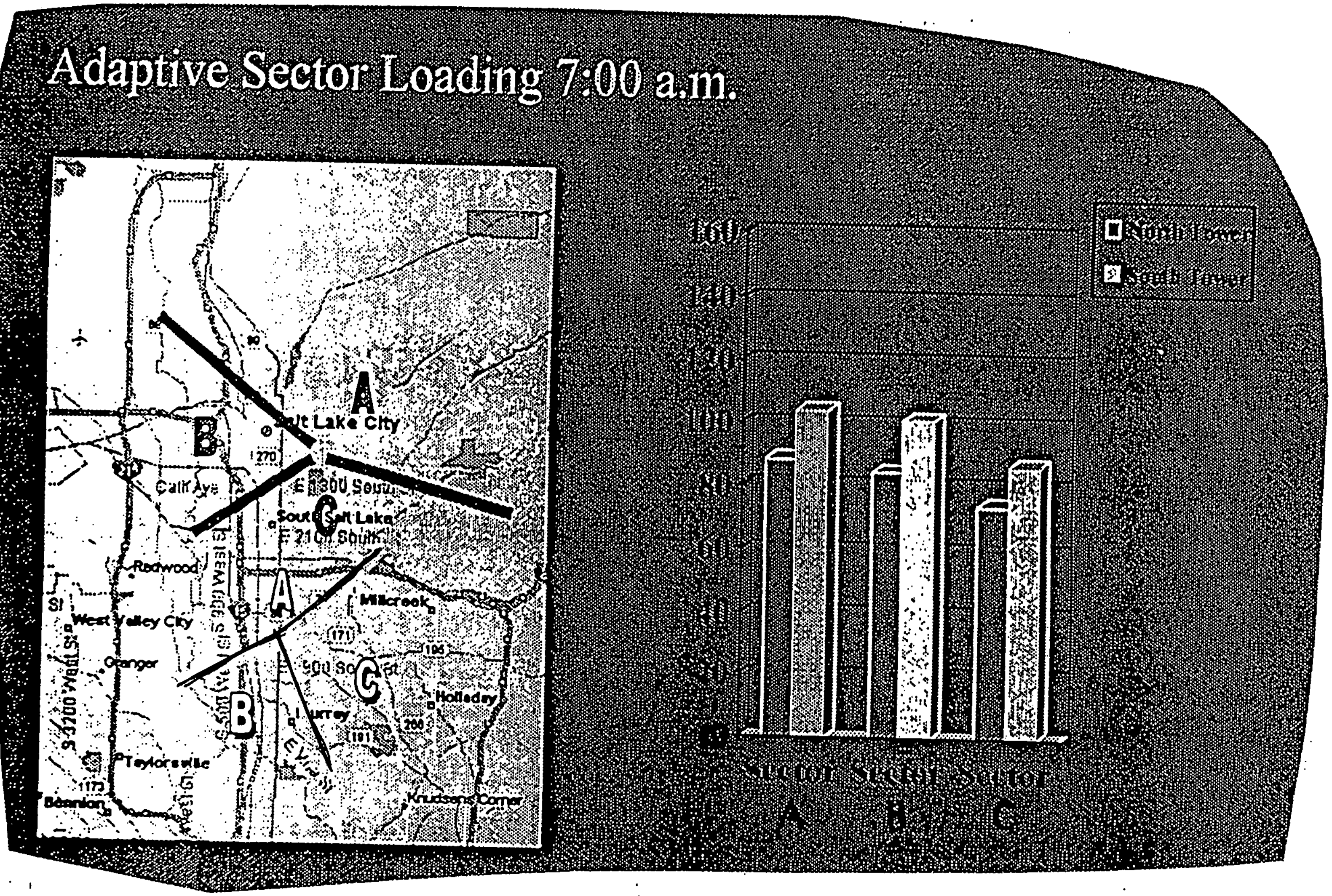

Sector Loading 5:00 p.m.
Salt Lake City
South Salt Lake
E 2100 South
Redwood
Millcreek
West Valley City
Granger
Holladay
Taylorsville
Knudsens Corner
A
B
C
160
140
120
100
80
60
40
20
0
North Tower
South Tower
Sector A
Sector B
Sector C

FIG. 83



Adaptive Sector Loading 7:00 a.m.
Millcreek
Holladay
Redwood
West Valley City
Granger
Taylorsville
Knudsens Corner
Bennion
160
140
100
80
South Tower
Sector
A
B
C

FIG. 84

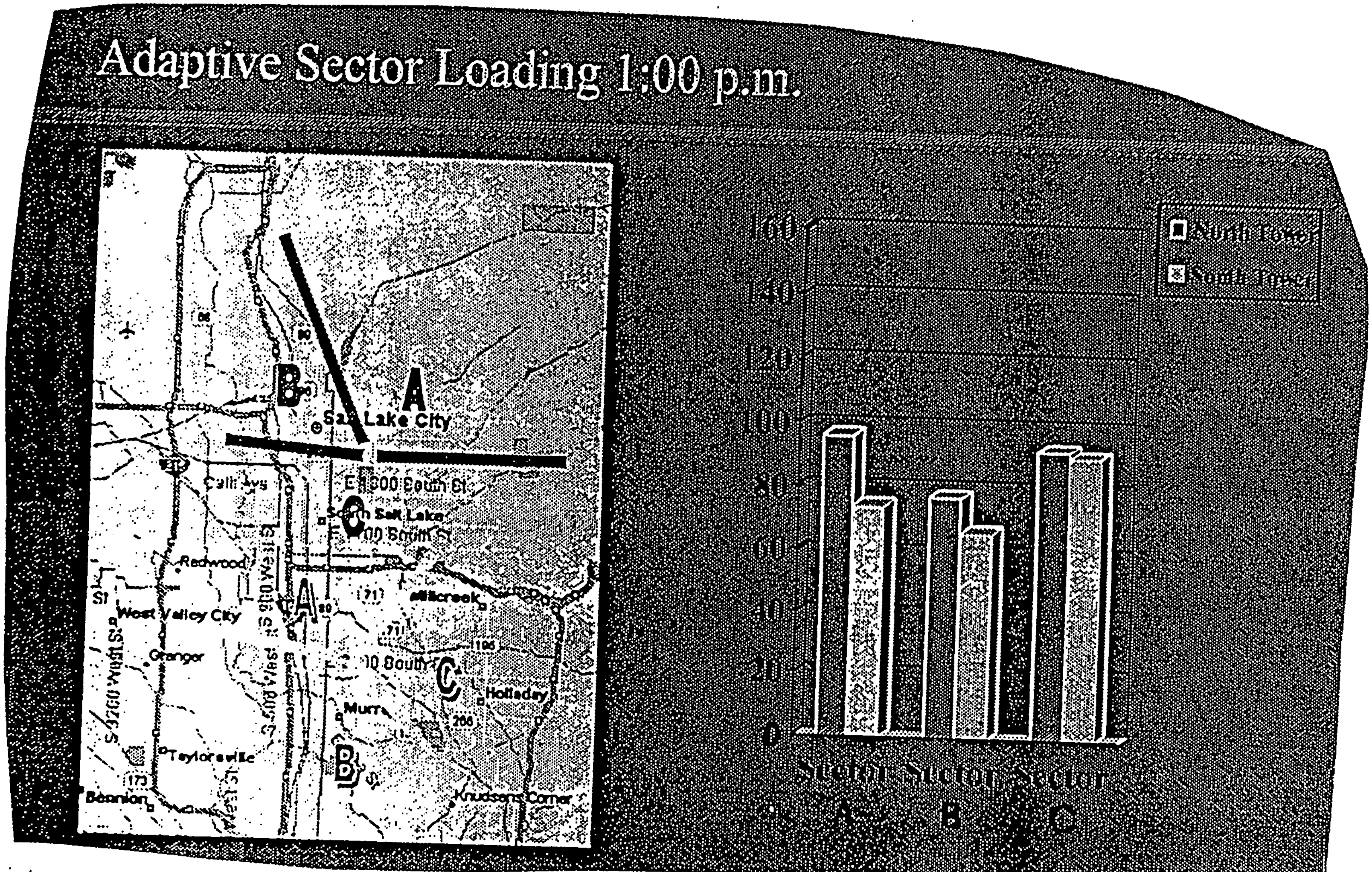

Adaptive Sector Loading 1:00 p.m.
A
B
C
Salt Lake City
South Salt Lake
Redwood
West Valley City
Granger
Taylorsville
Bennion
Millcreek
Holladay
Murray
Knudsens Corner
160
140
120
100
80
60
40
20
0
North Tower
South Tower
Sector A
Sector B
Sector C

FIG. 85

006090"55606560

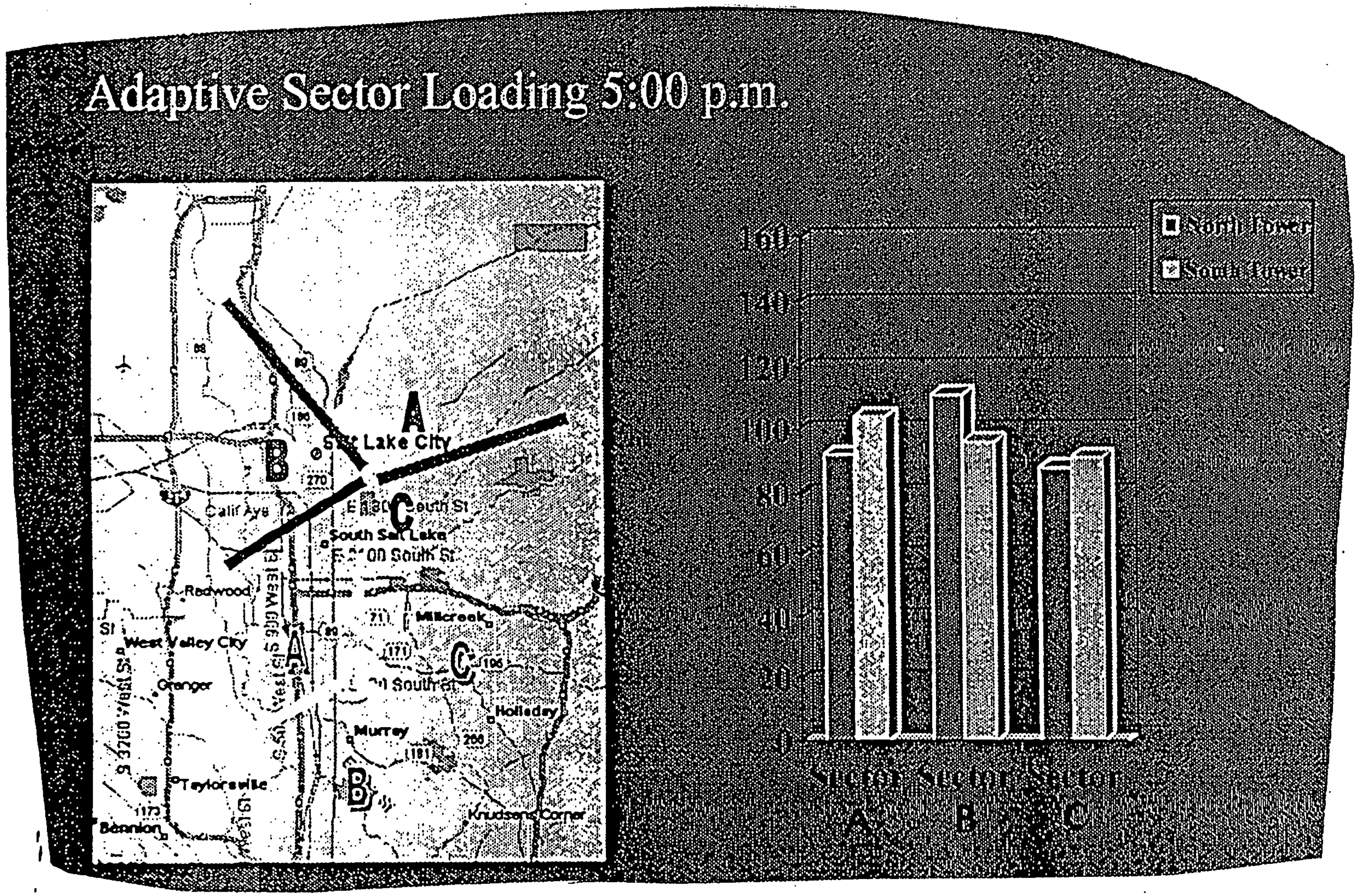


FIG. 86

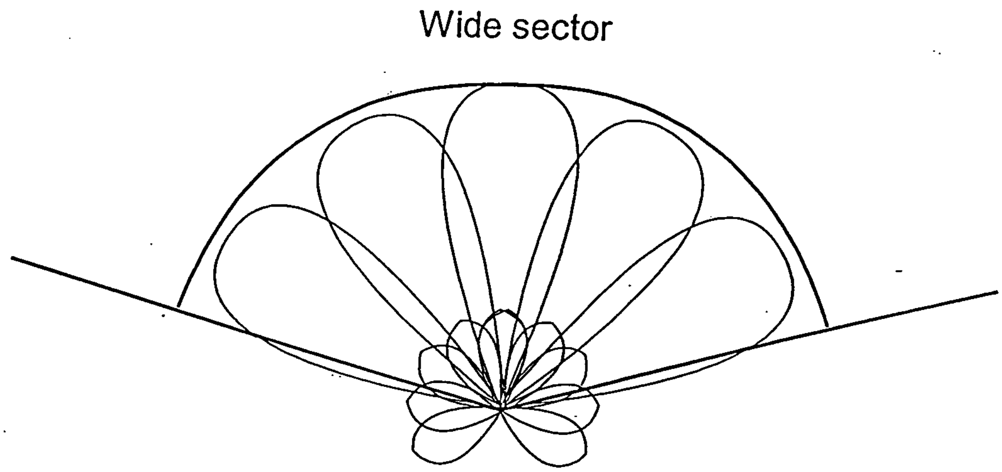


FIG. 87A

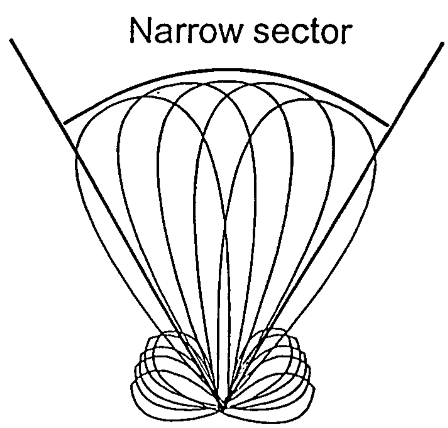
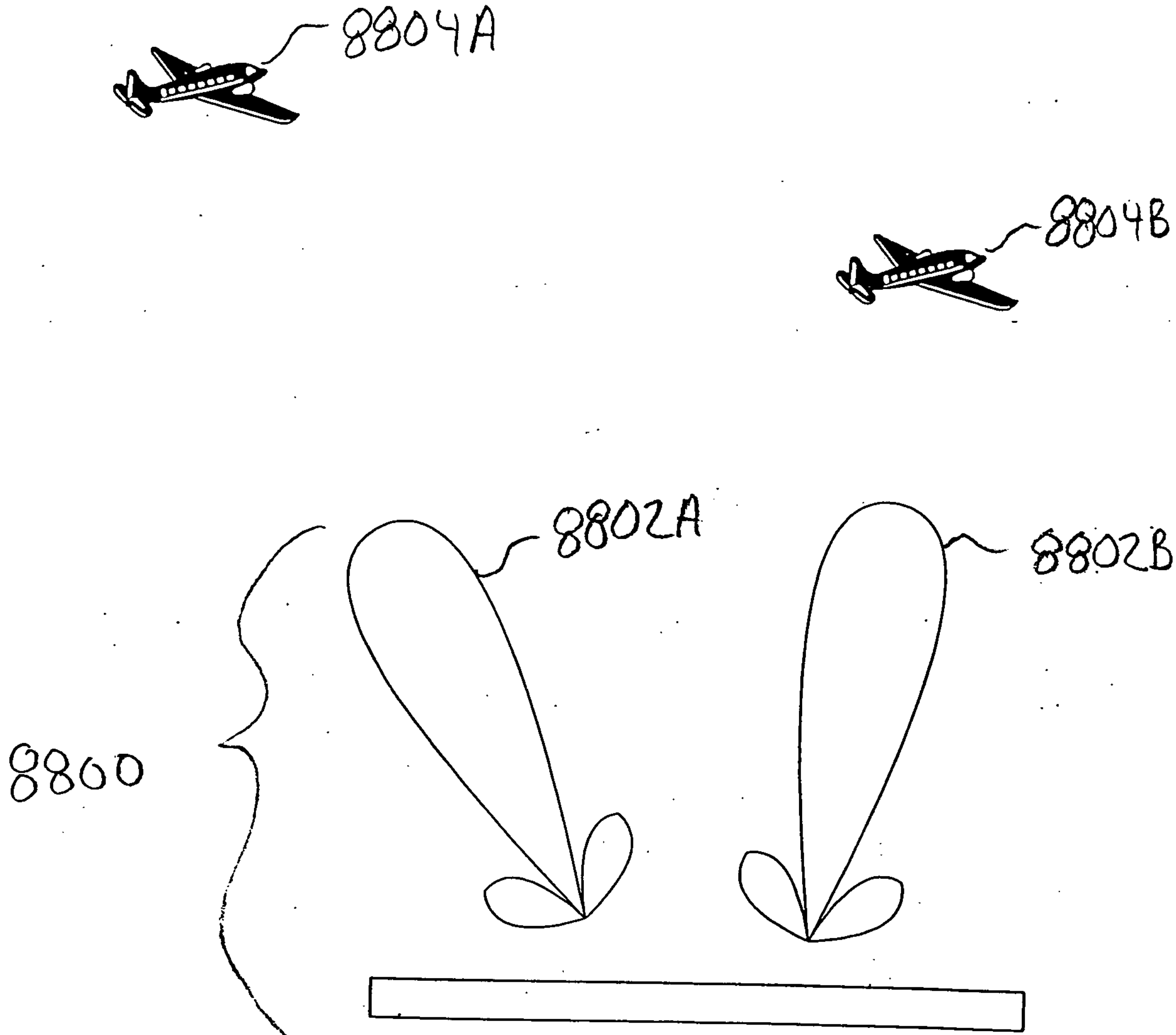


FIG. 87B



Phased array with multiple tracking main beams

FIG. 88

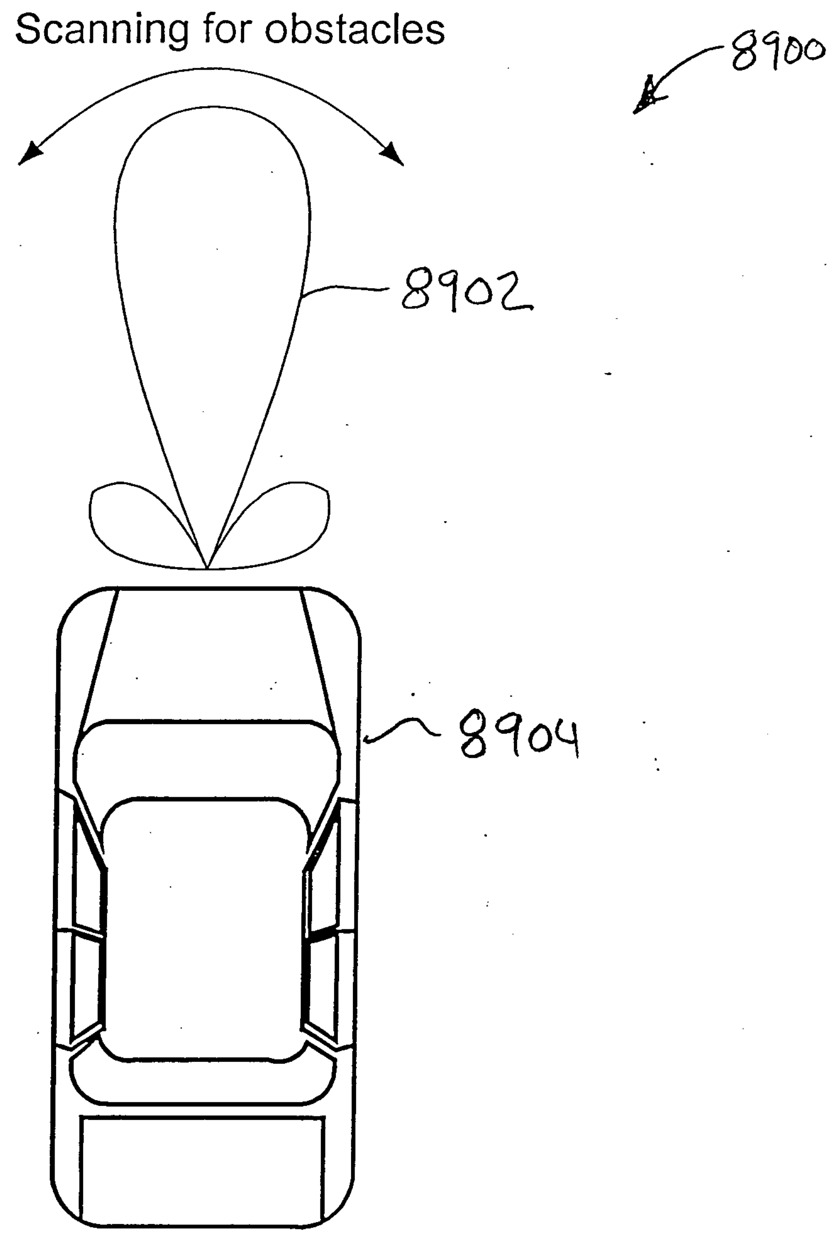


FIG. 89

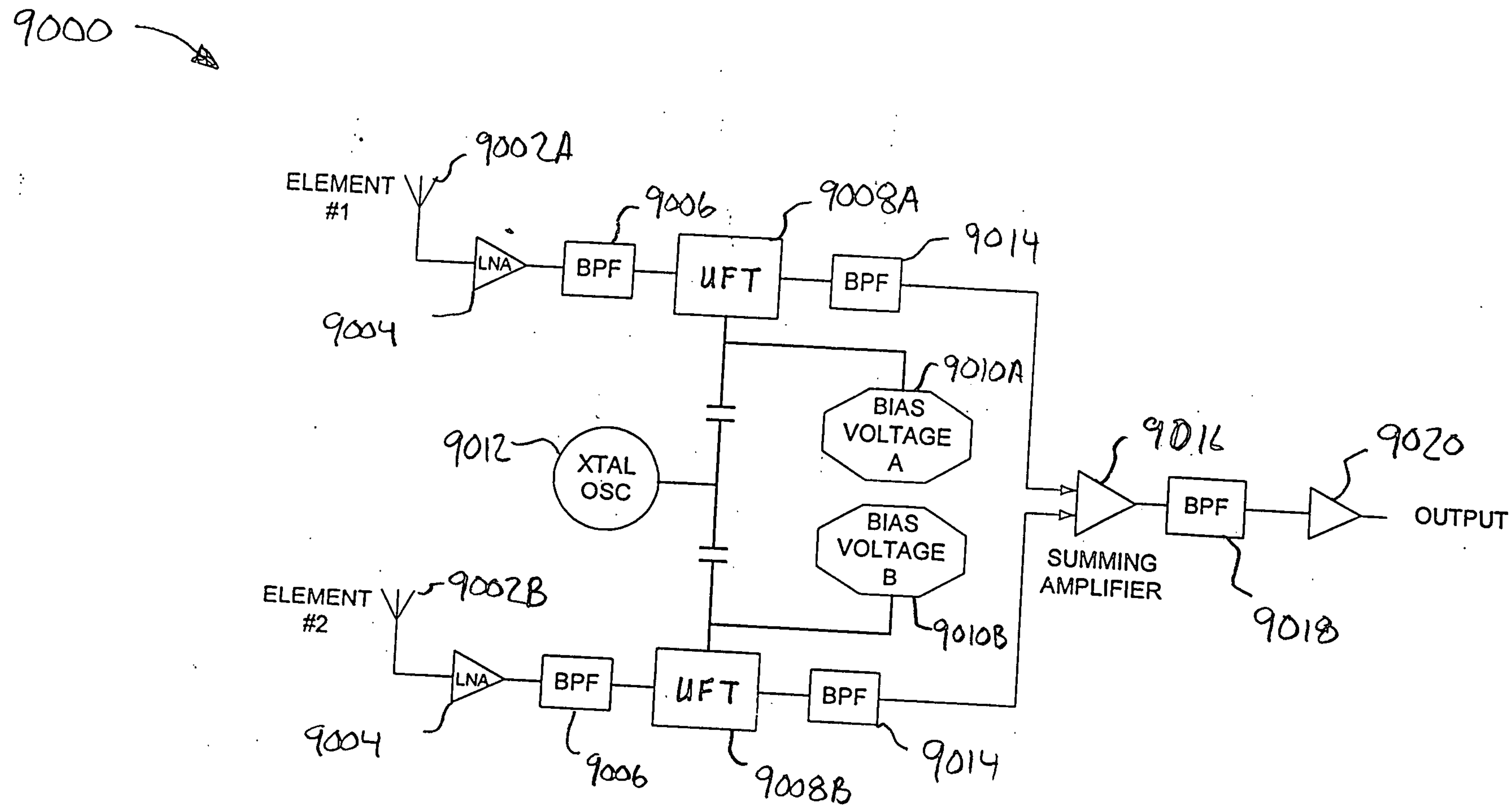

9000
ELEMENT #1
9002A
9004
LNA
BPF
9006
UFT
9008A
BPF
9014
9010A
BIAS VOLTAGE A
9012
XTAL OSC
BIAS VOLTAGE B
9010B
ELEMENT #2
9002B
9004
LNA
BPF
9006
UFT
9008B
BPF
9014
9016
SUMMING AMPLIFIER
BPF
9018
9020
OUTPUT

FIG. 90A

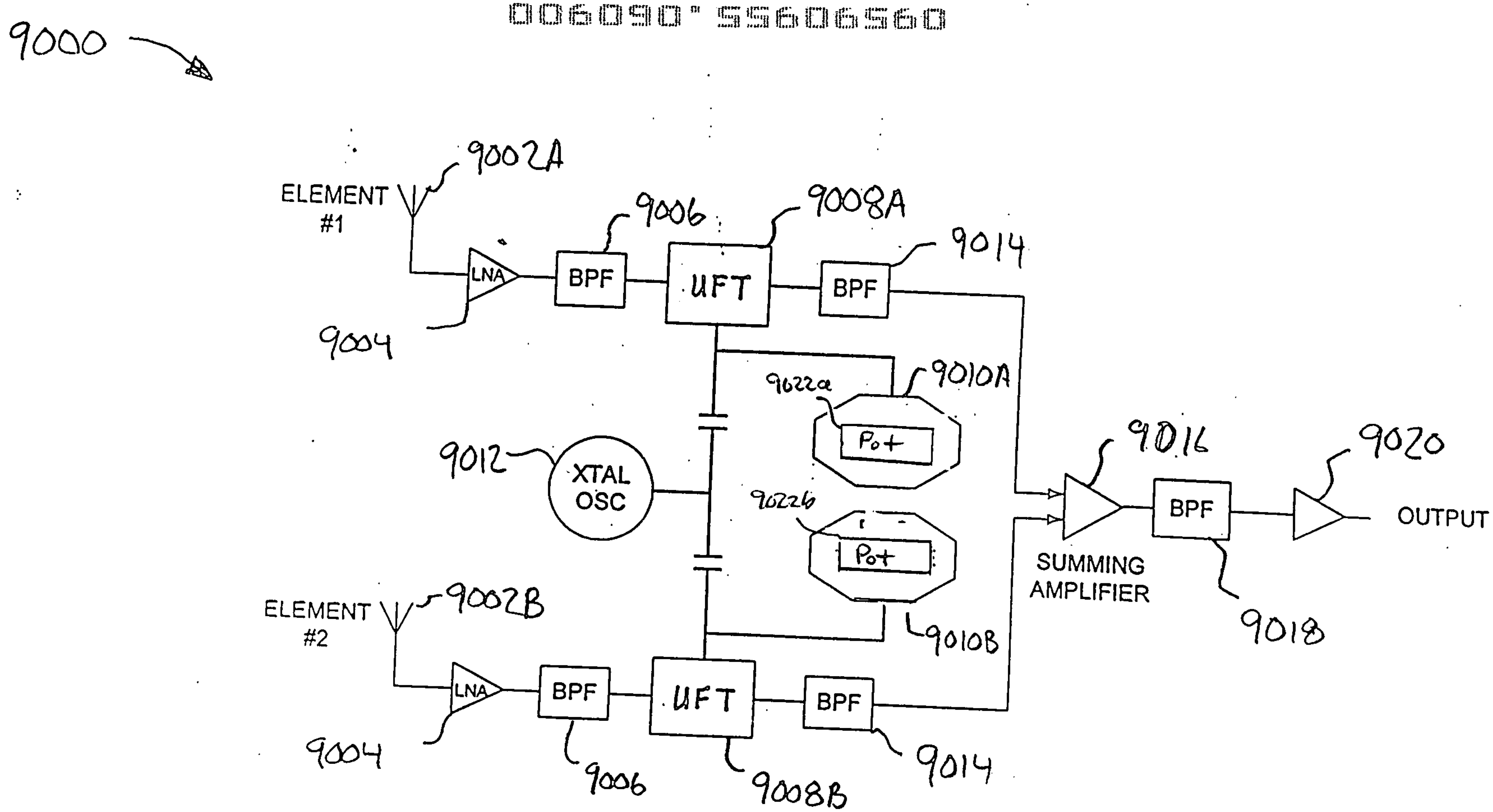

9000
ELEMENT #1
9002A
9004
LNA
BPF
9006
UFT
9008A
BPF
9014
9010A
9022a
Po+
9012
XTAL OSC
9022b
Po+
9010B
ELEMENT #2
9002B
9004
LNA
BPF
9006
UFT
9008B
BPF
9014
9016
SUMMING AMPLIFIER
BPF
9018
9020
OUTPUT

FIG. 90B

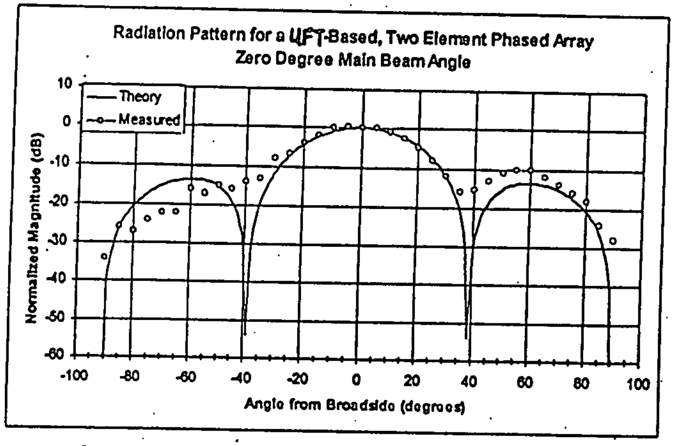


FIG. 91A *0 degree scan angle.*

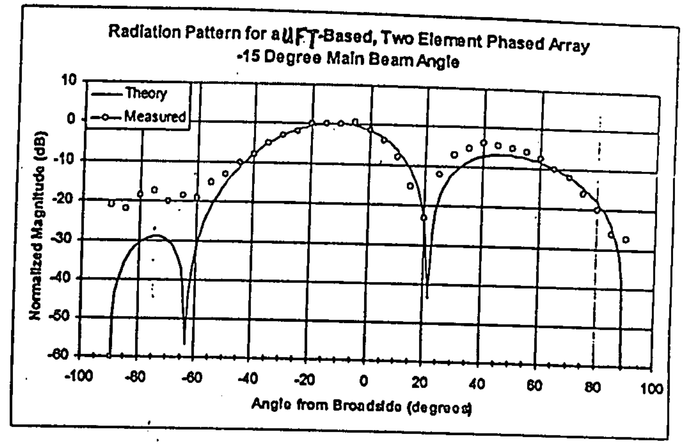


FIG. 91B *-15 degree scan angle.*

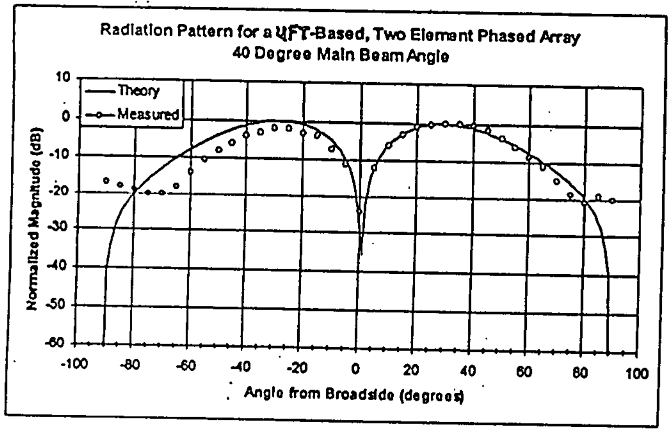


FIG. 91C *40 degree scan angle.*

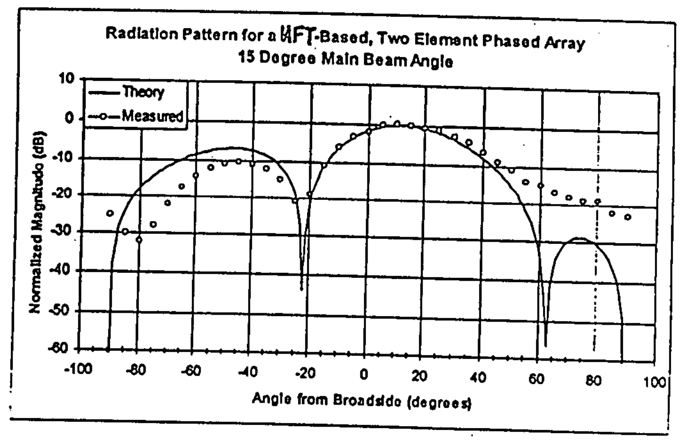


FIG. 91D *15 degree scan angle.*

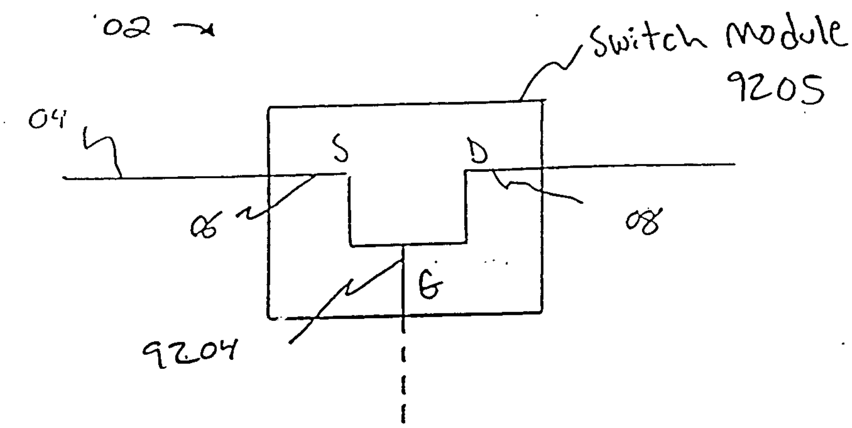


FIG. 92A

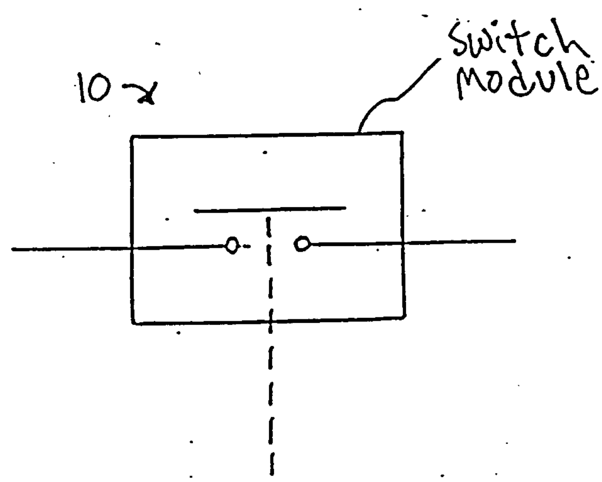


FIG. 92B

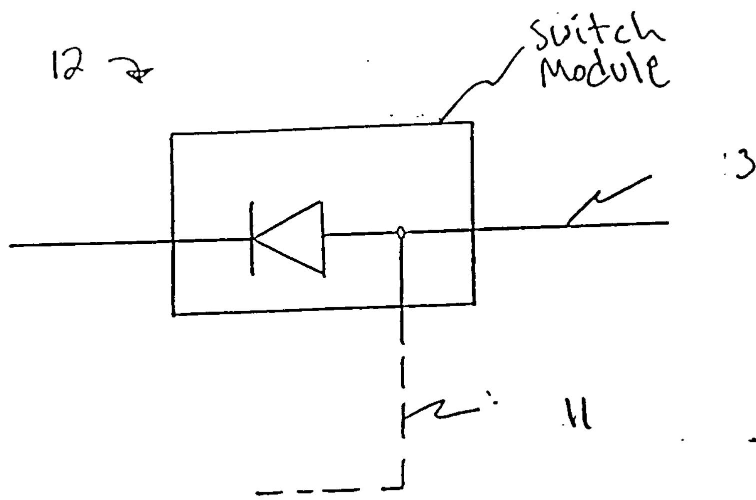


FIG. 92C

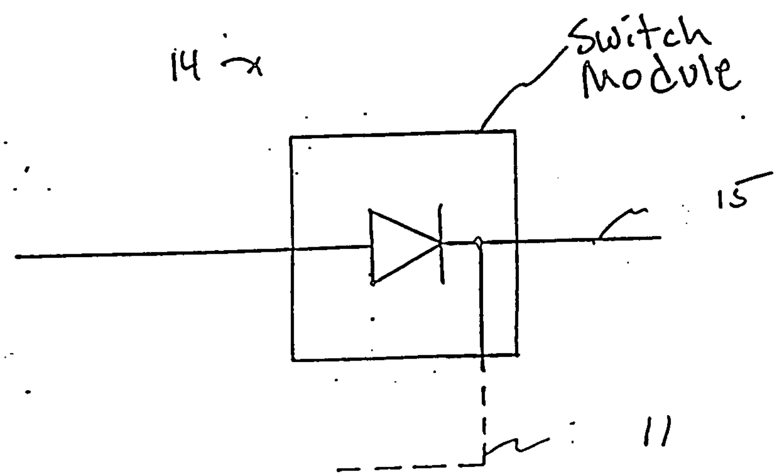
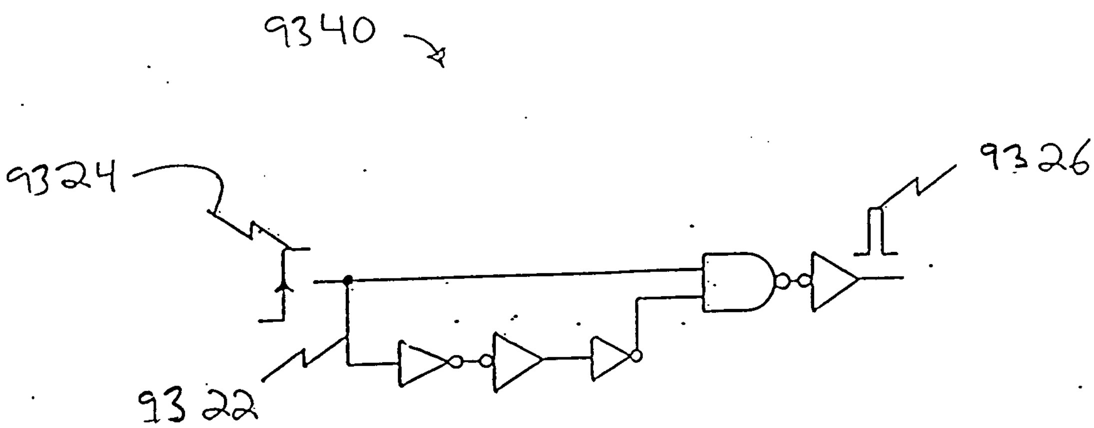
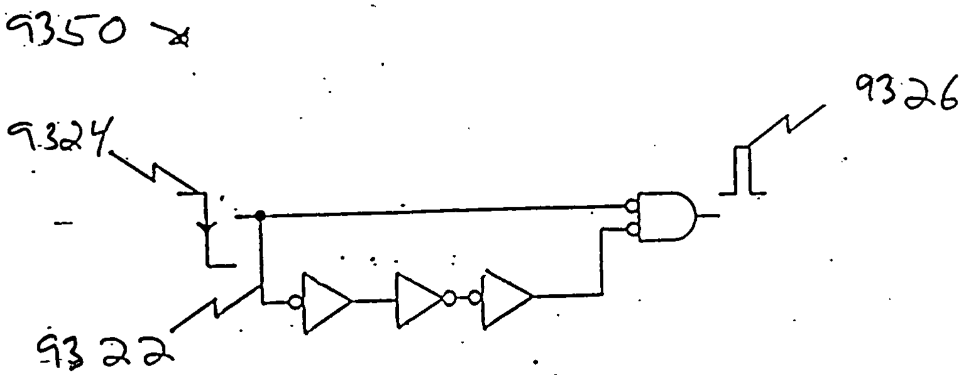


FIG. 92D



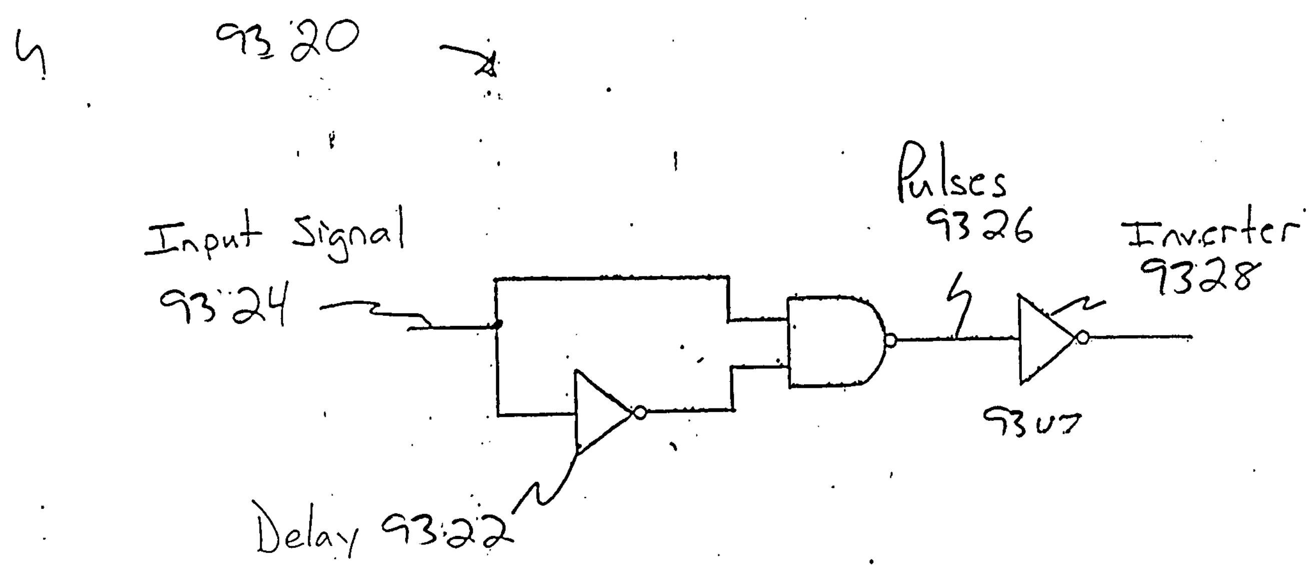
A. rising edge pulse generator

FIG. 93A



B. falling-edge pulse generator

FIG. 93B



-substantial equivalence in logic only is necessary.
-u7 shown for polarity consistency with
ckt examples described elsewhere.

FIG 93C

5

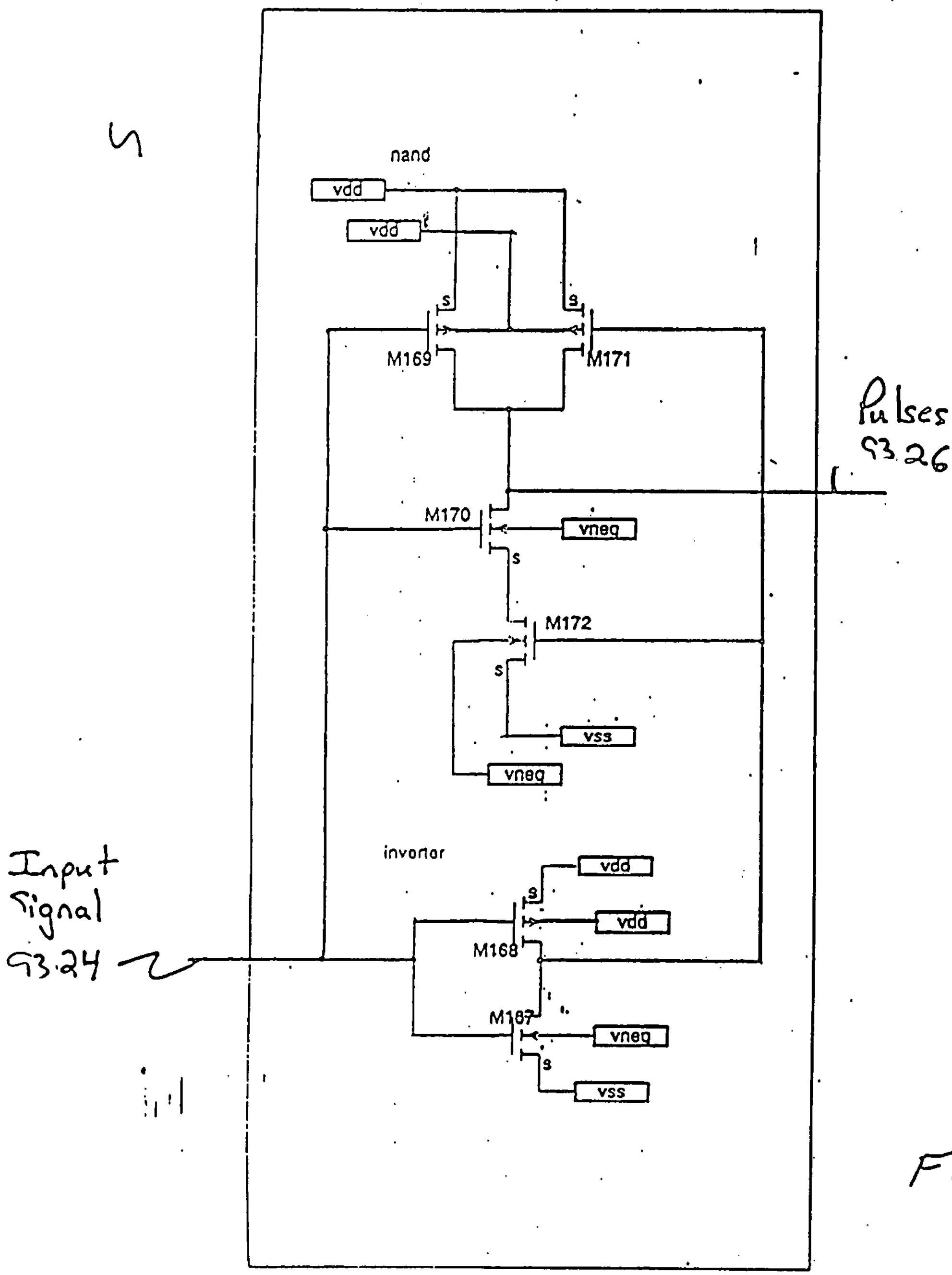


FIG 93D

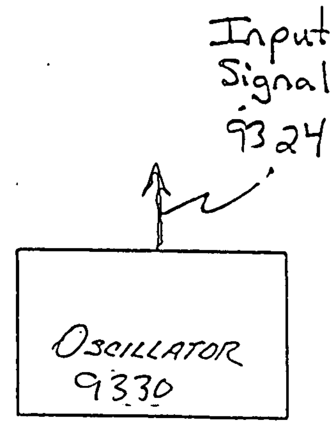


FIG. 93E

9401

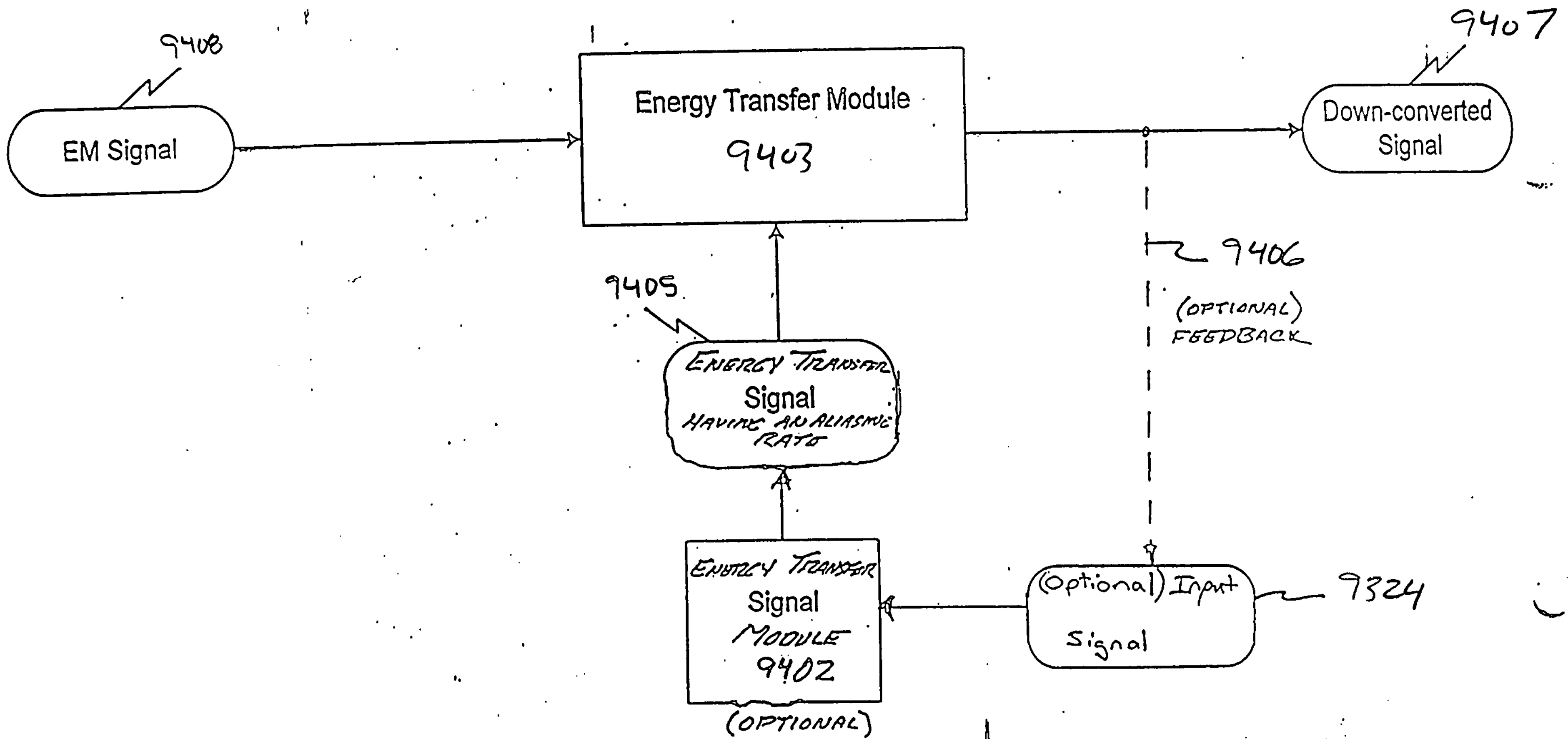


FIG. 94

9807-10.rtd/34

5

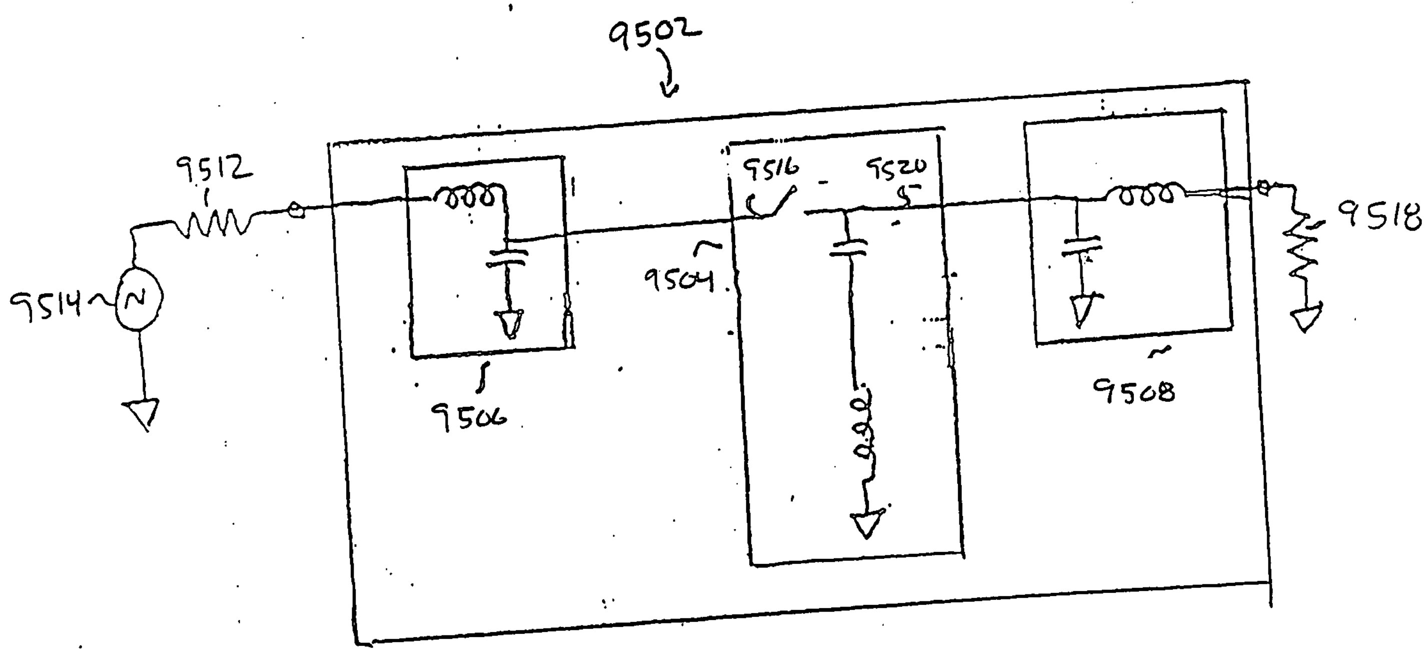


Fig 95 - Impedance Matched Aliasing Module

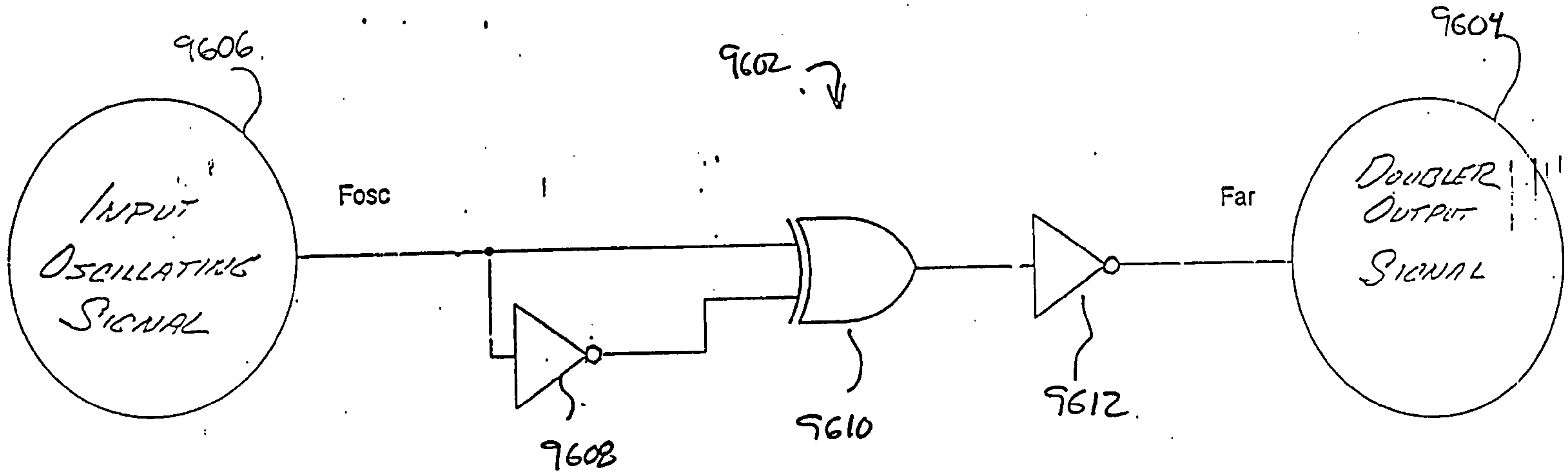

9606
INPUT
OSCILLATING
SIGNAL
Fosc
9602
9608
9610
9612
Far
9604
DOUBLER
OUTPUT
SIGNAL

FIG. 96A

00609055606560

FIG. 96B

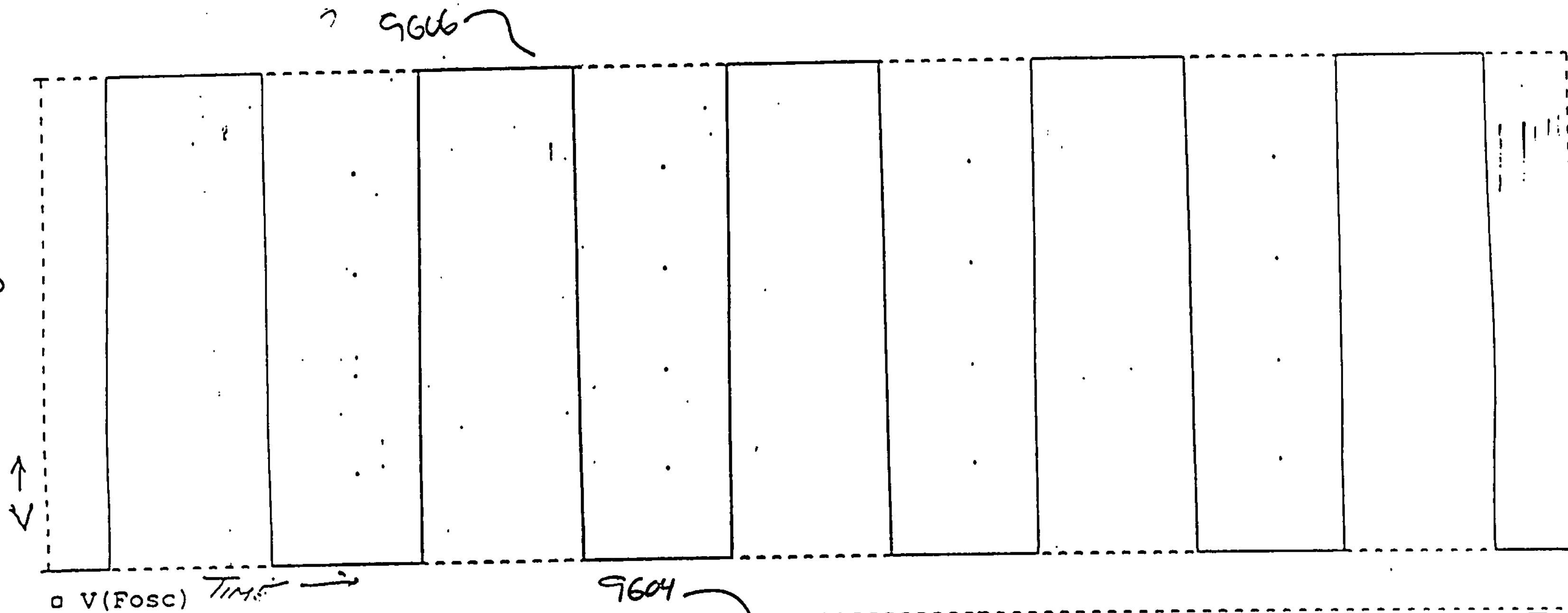
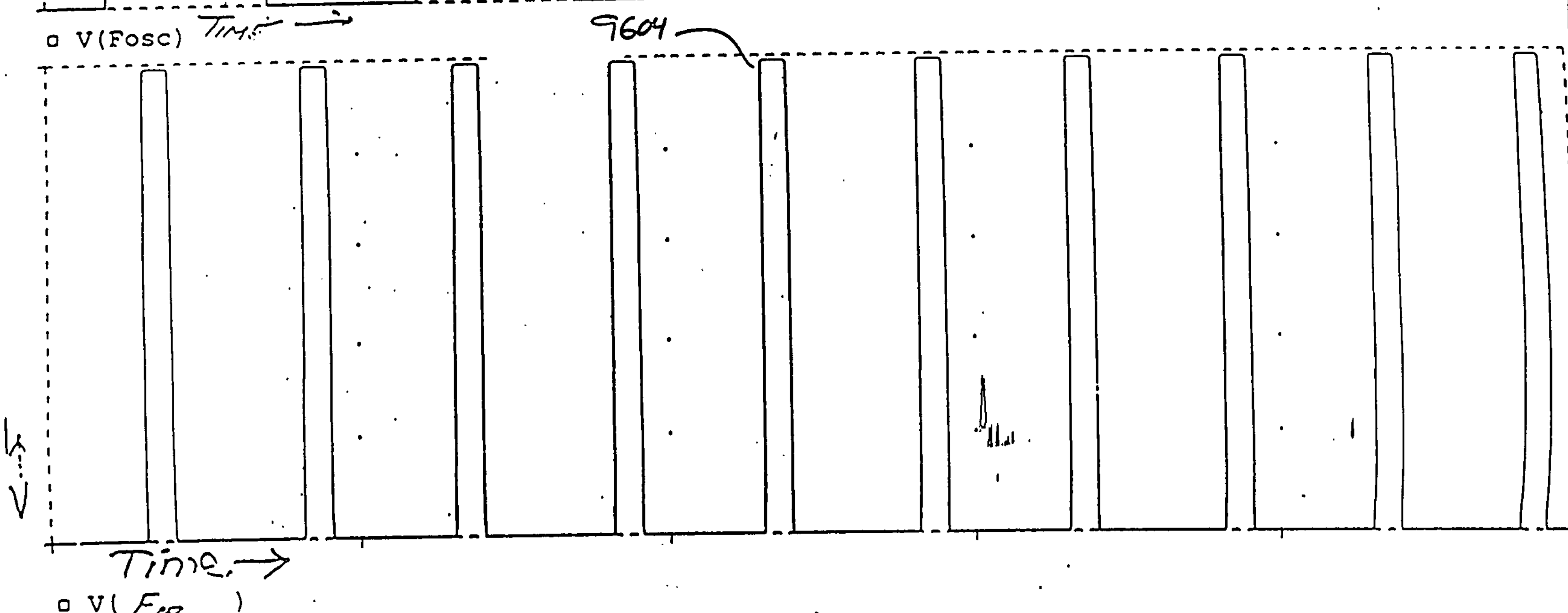


FIG. 96C



Time

Date: October 12, 1998

Page 1

Time: 17:23:38

00609055.006090

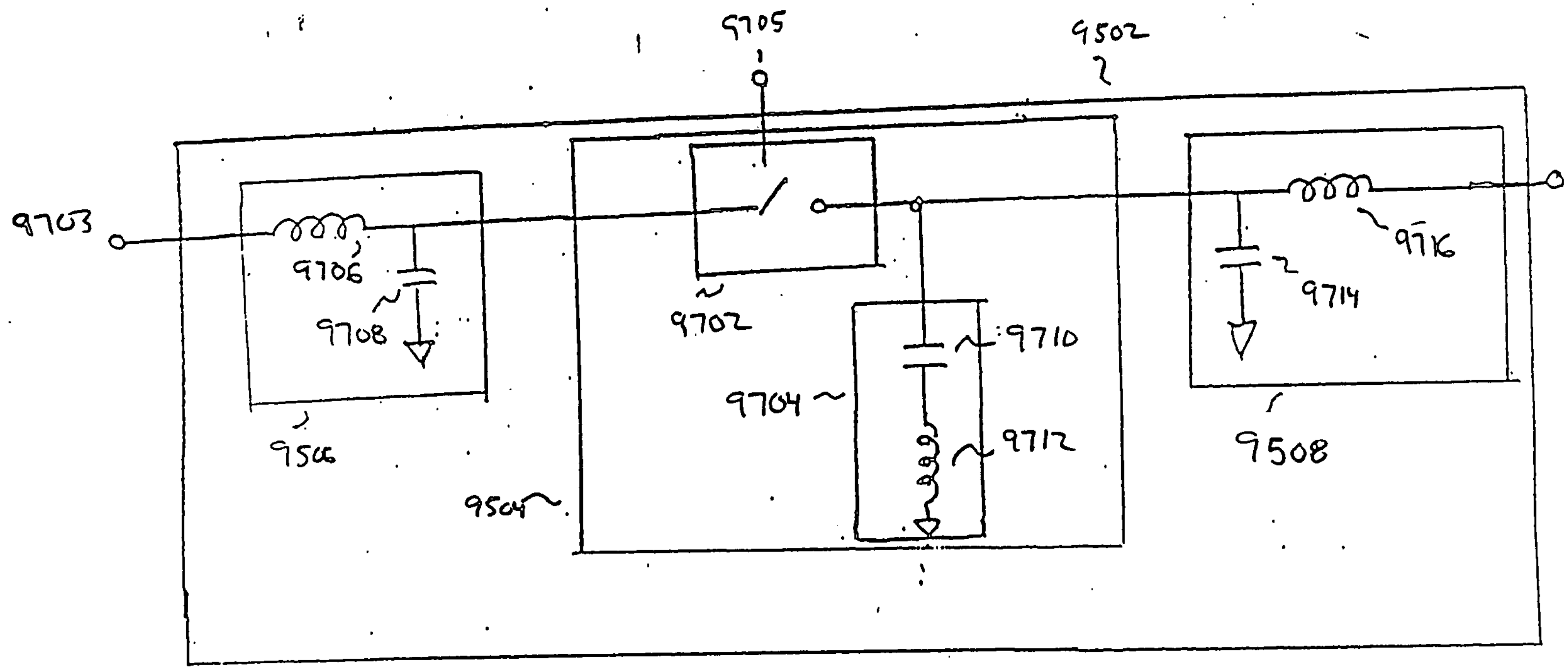


Fig 97 - Aliasing Module

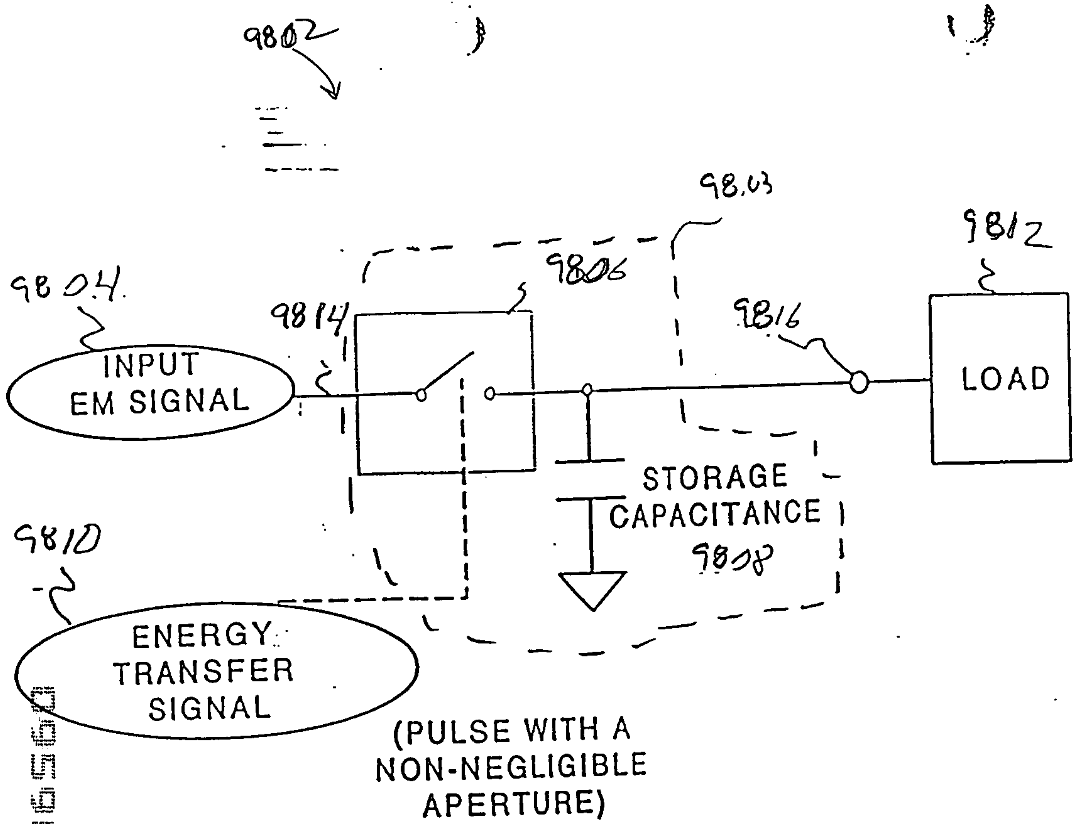


FIG 98A

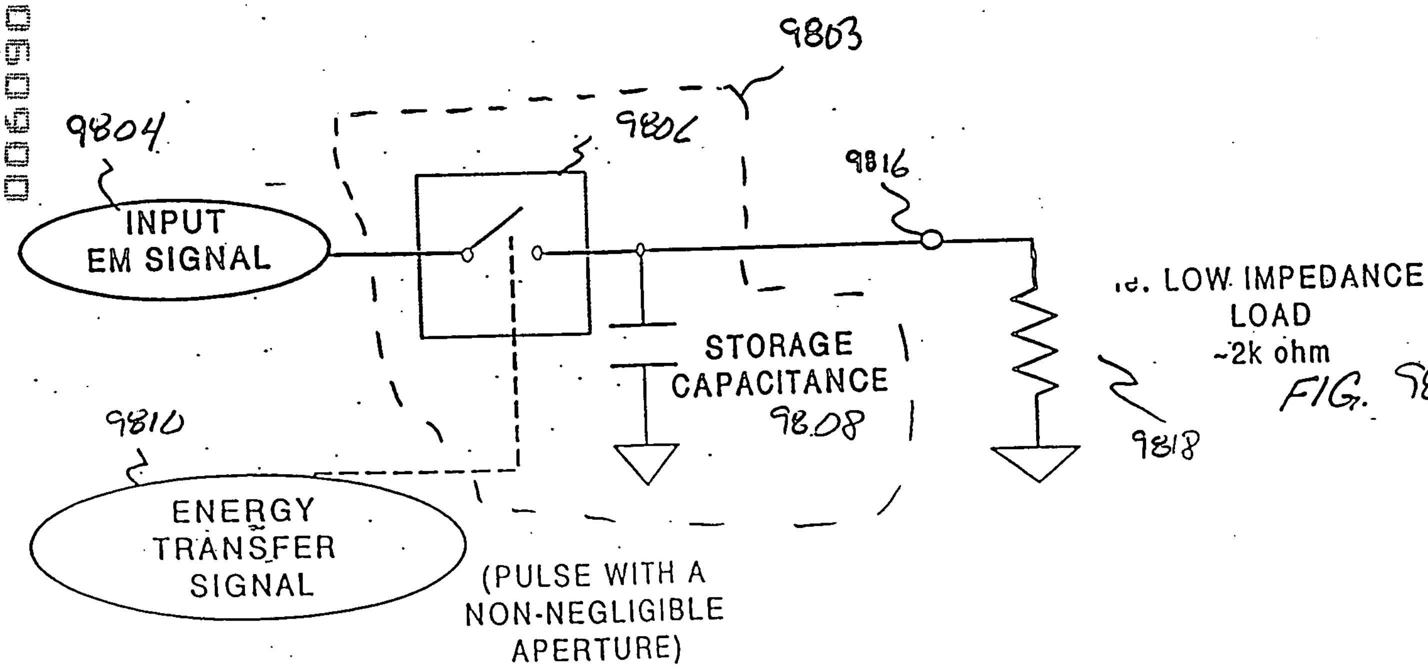


FIG. 98B

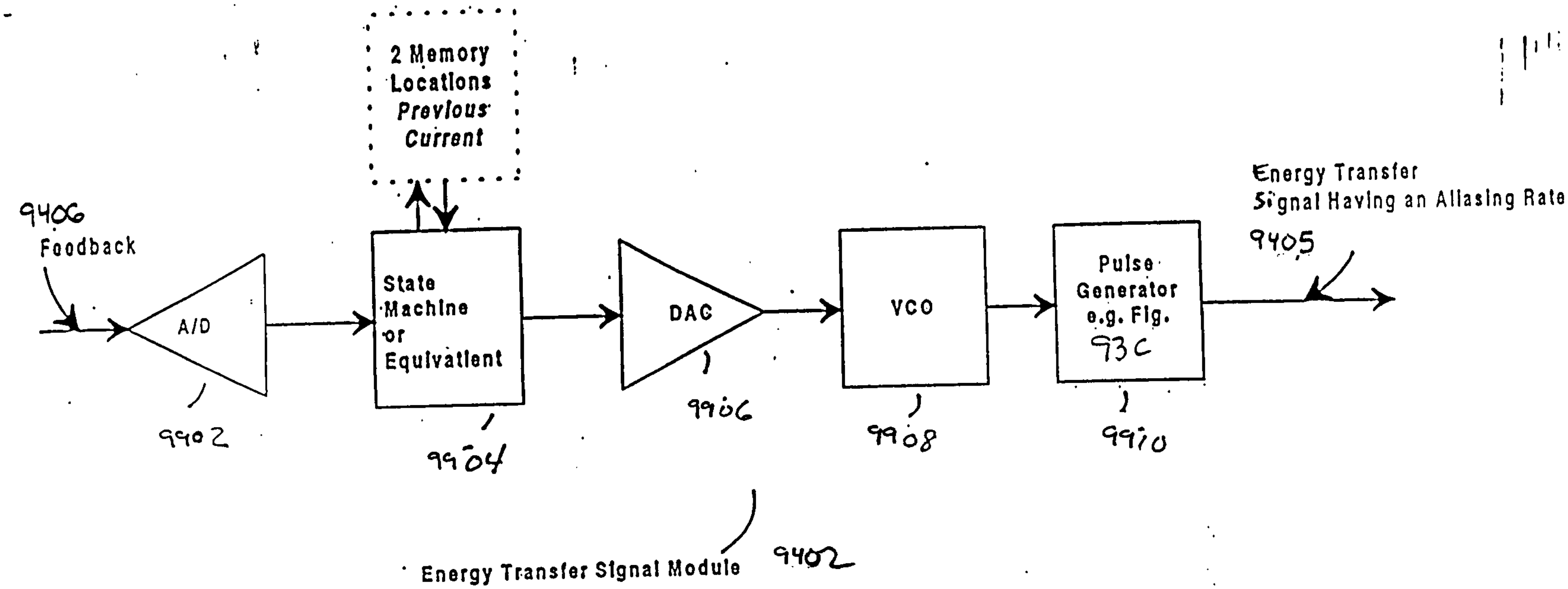
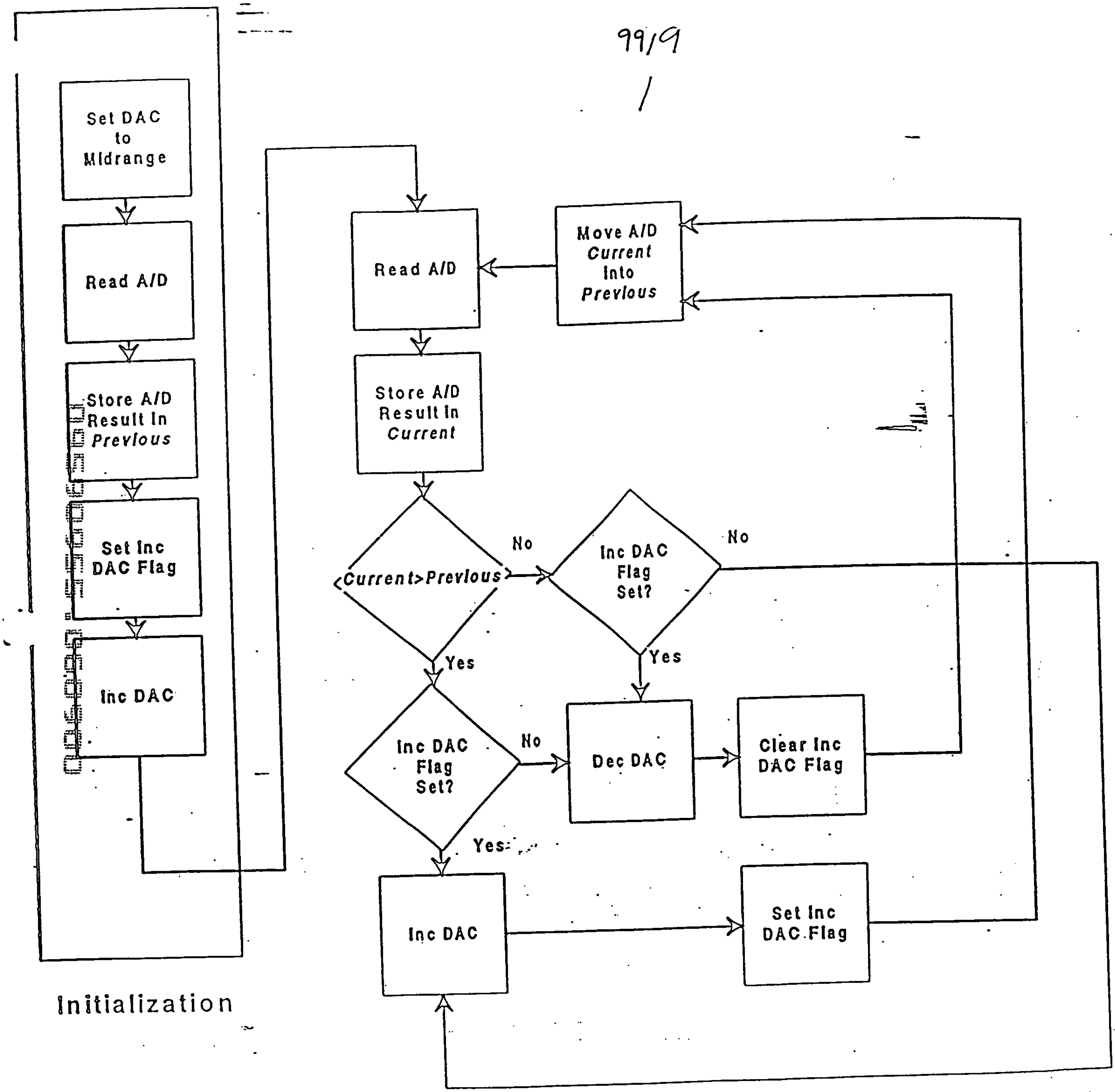

2 Memory Locations Previous Current
9406
Foodback
A/D
9902
State Machine or Equivalent
9904
DAC
9906
VCO
9908
Pulse Generator e.g. Fig. 93C
9910
Energy Transfer Signal Having an Aliasing Rate
9405
Energy Transfer Signal Module
9402

FIG. 99A

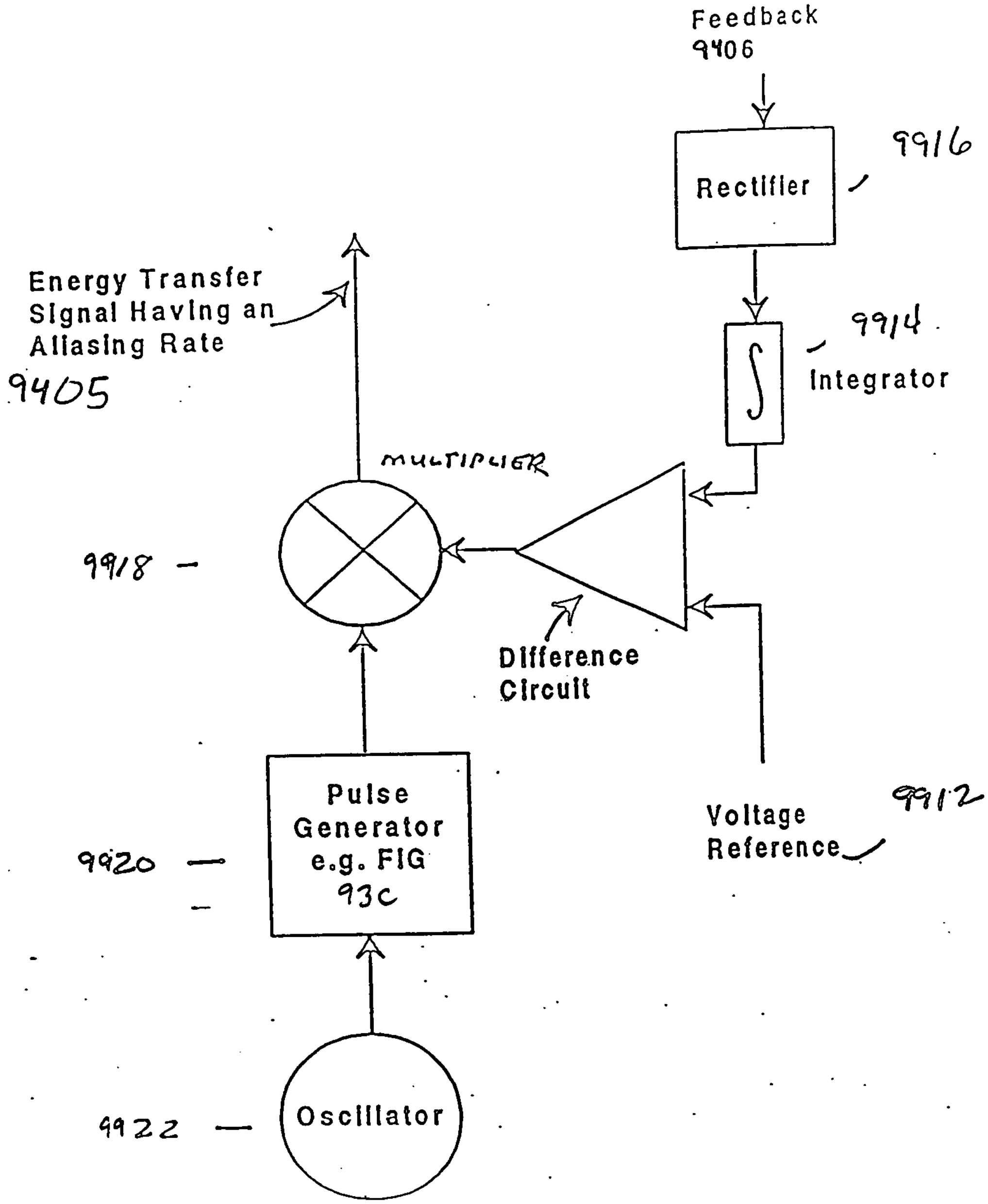
99/9



State Machine Flowchart

FIG. 99B

9203



Energy Transfer Signal Module 9402

FIG. 99C

00609055 095609

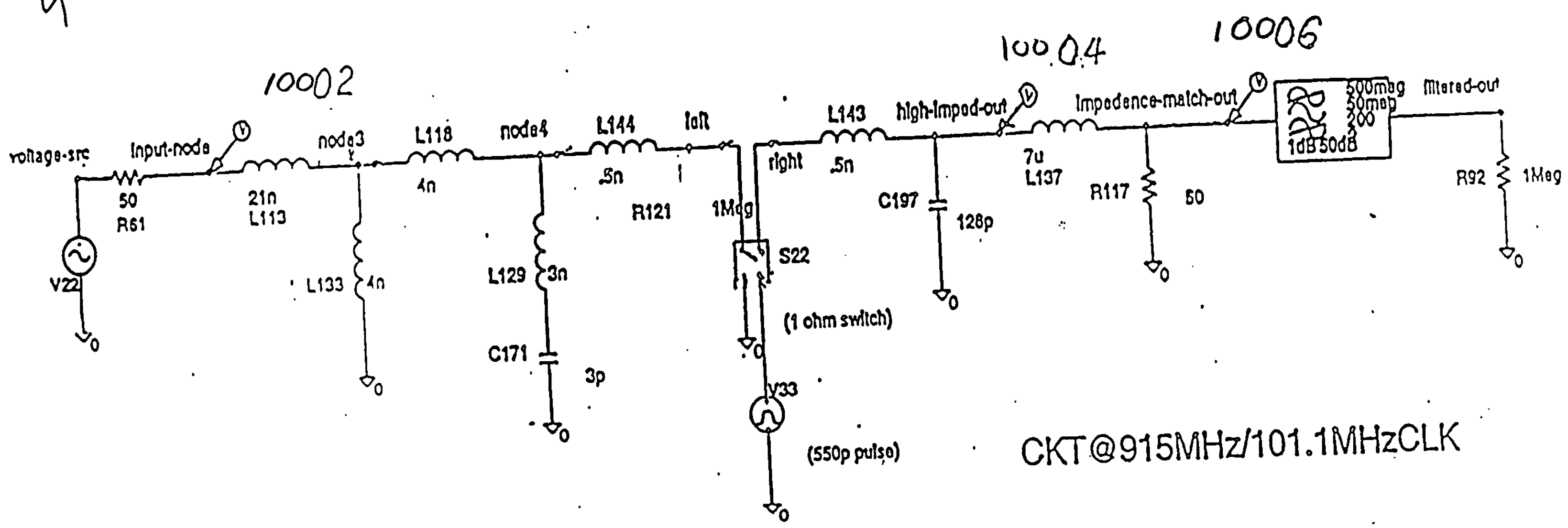
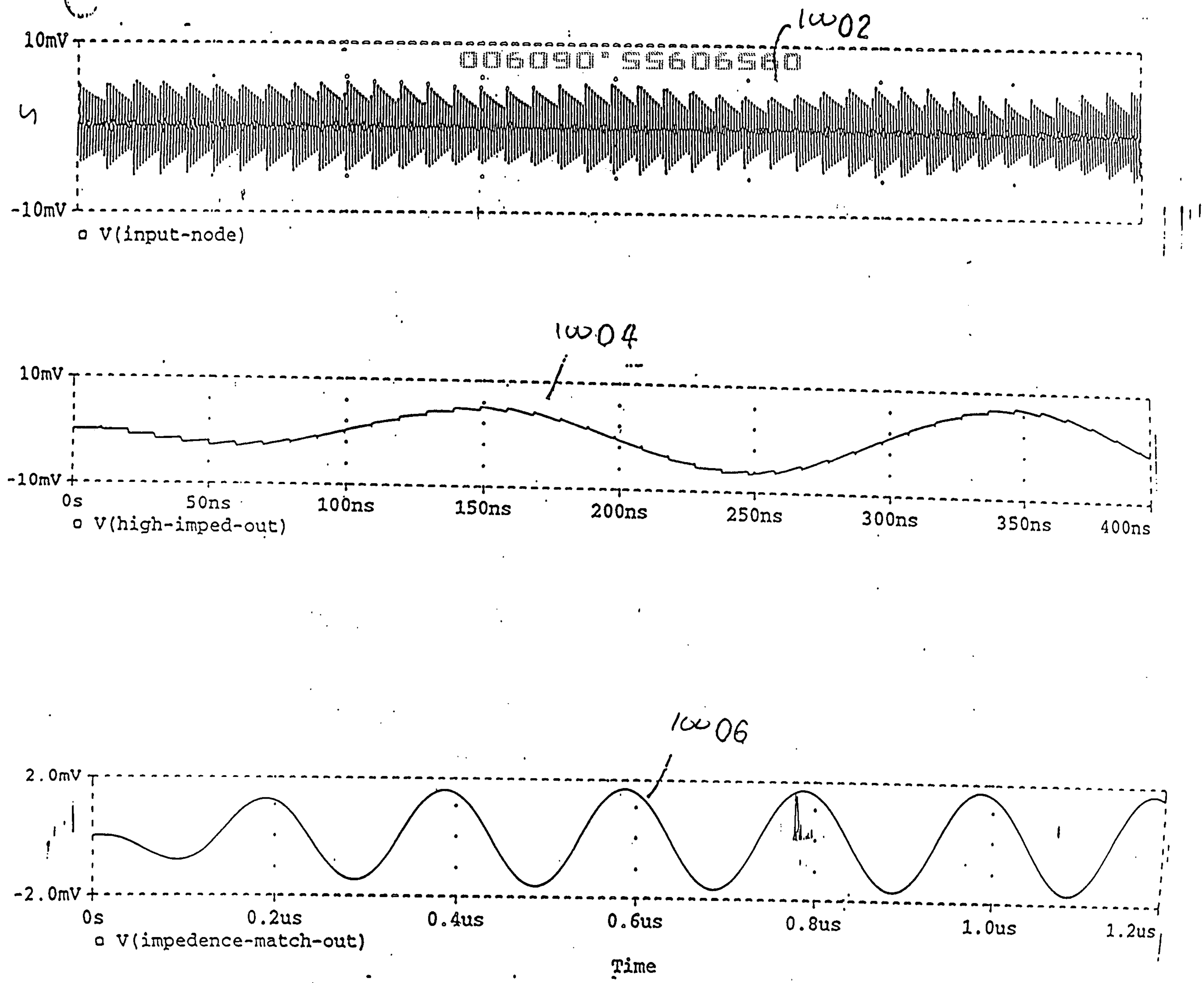


Fig. 100



1w02
10mV
-10mV
V(input-node)
1w04
10mV
-10mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V(high-imped-out)
1w06
2.0mV
-2.0mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
V(impedence-match-out)
Time

Fig. 1c7

006090"SS606S60

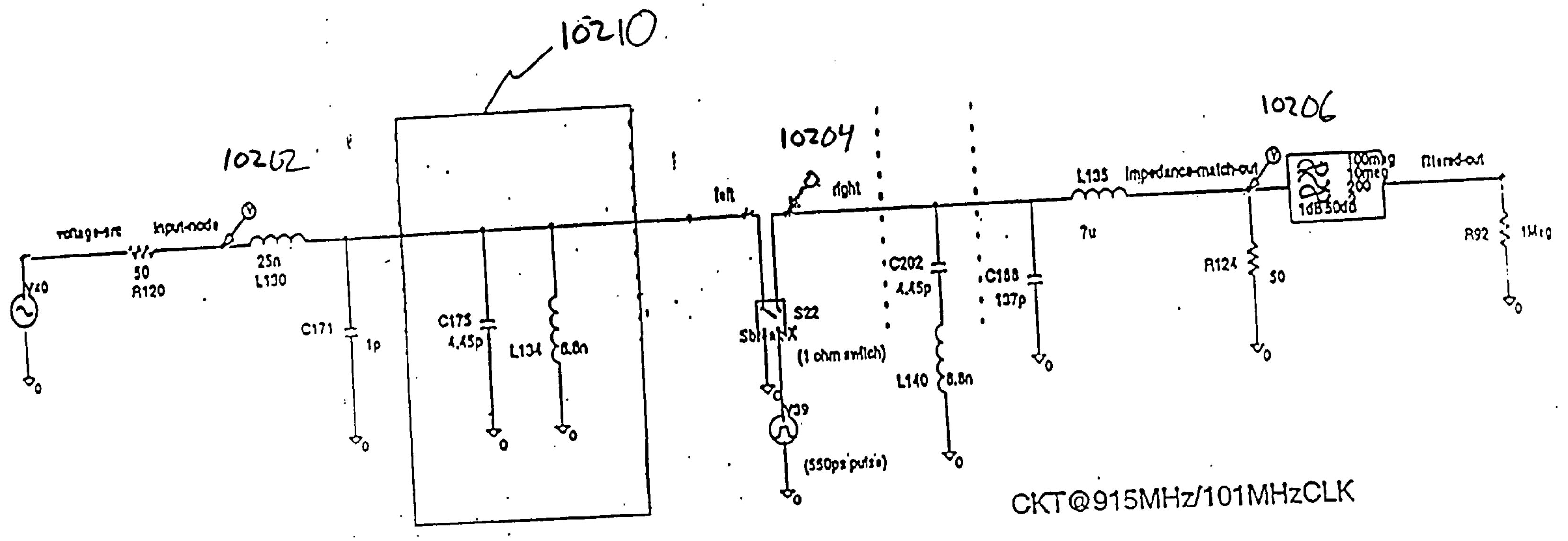


Fig. 102

00609055606560

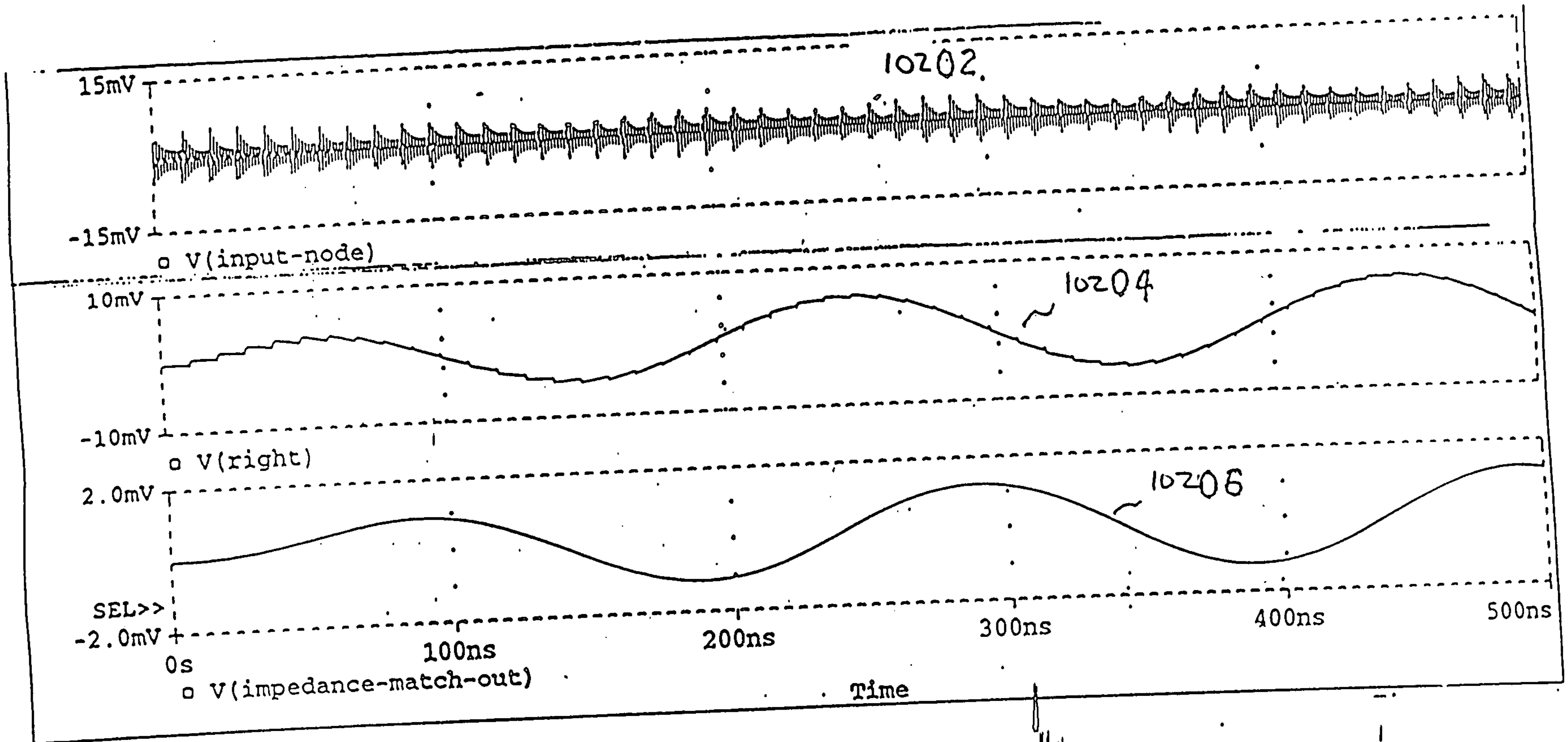


Fig 103

009090"SS606S60

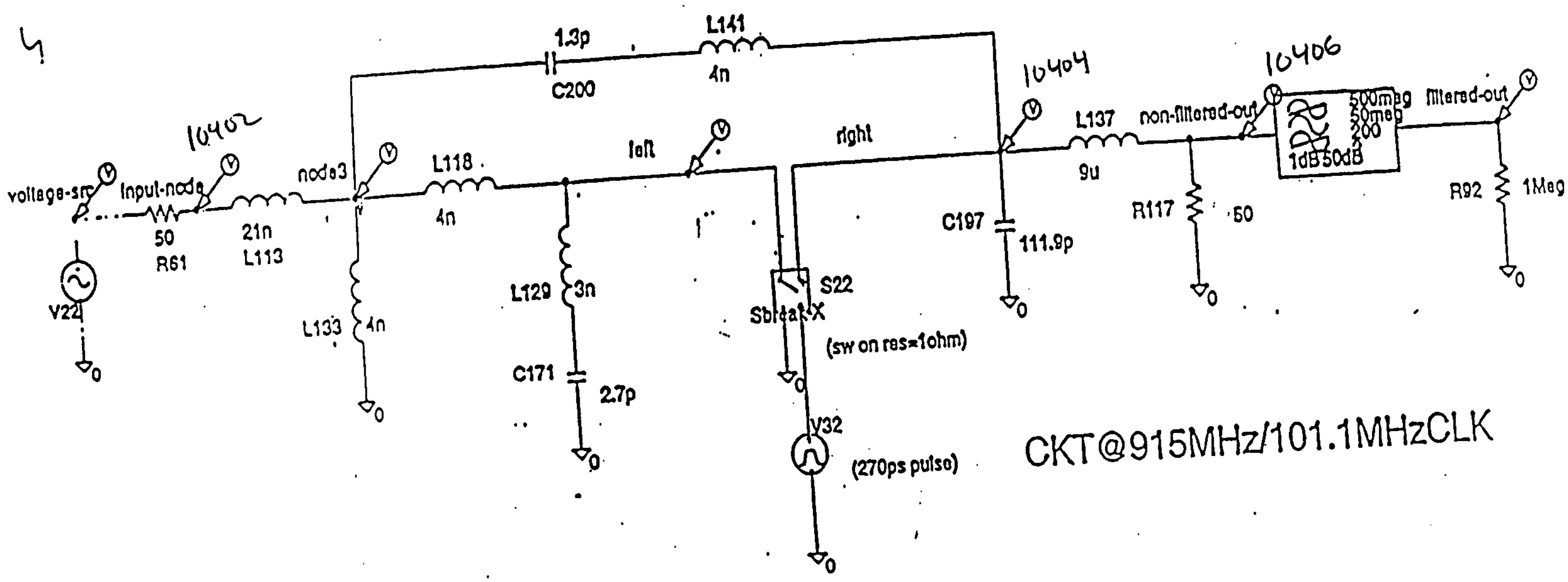


Fig: 104

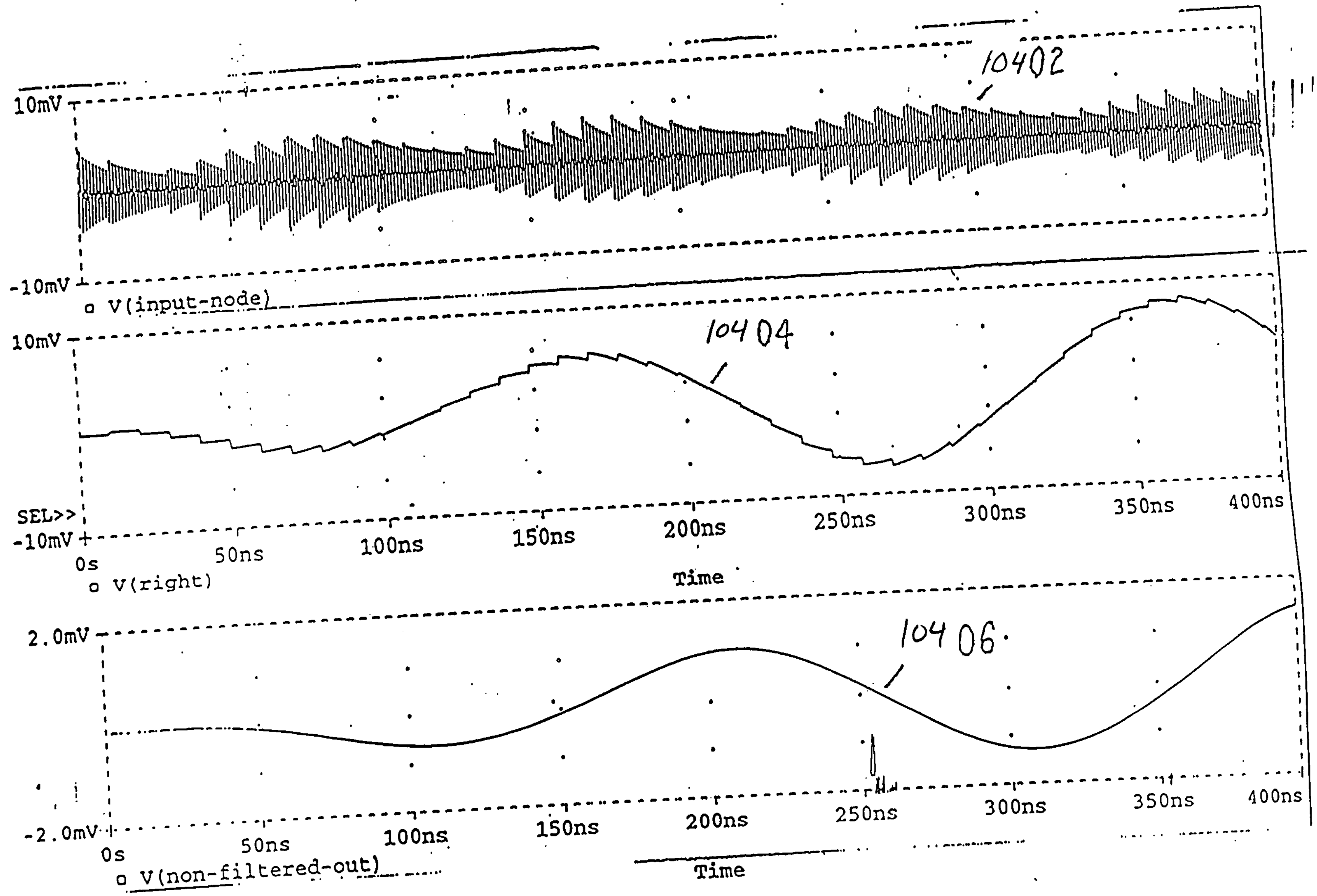

10mV
-10mV
V(input-node)
10402
10mV
SEL>>
-10mV
10404
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
Time
V(right)
2.0mV
-2.0mV
10406
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
Time
V(non-filtered-out)

Fig. 105

006090" 55606560

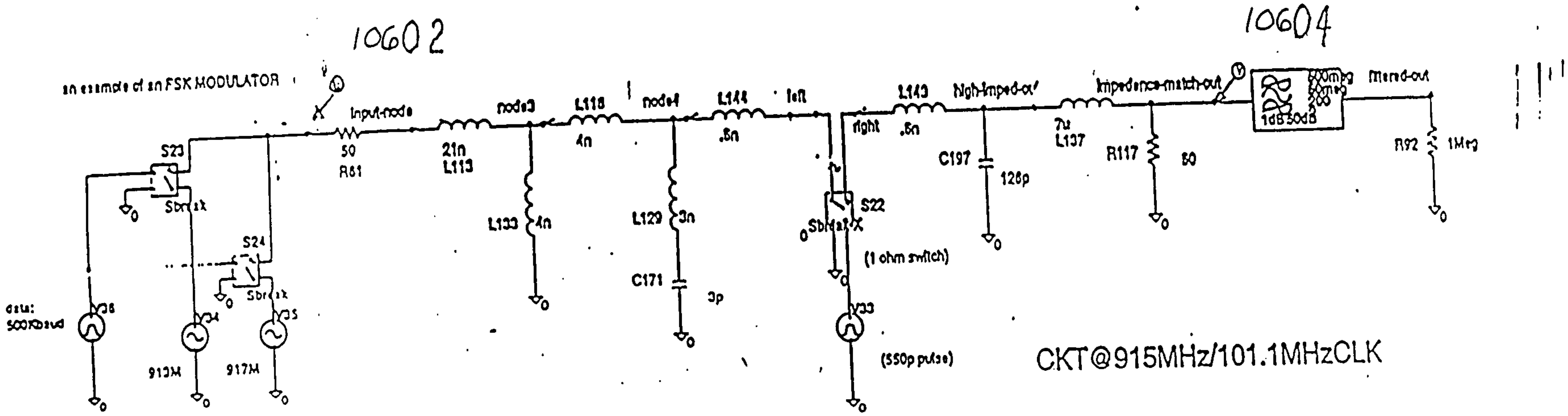
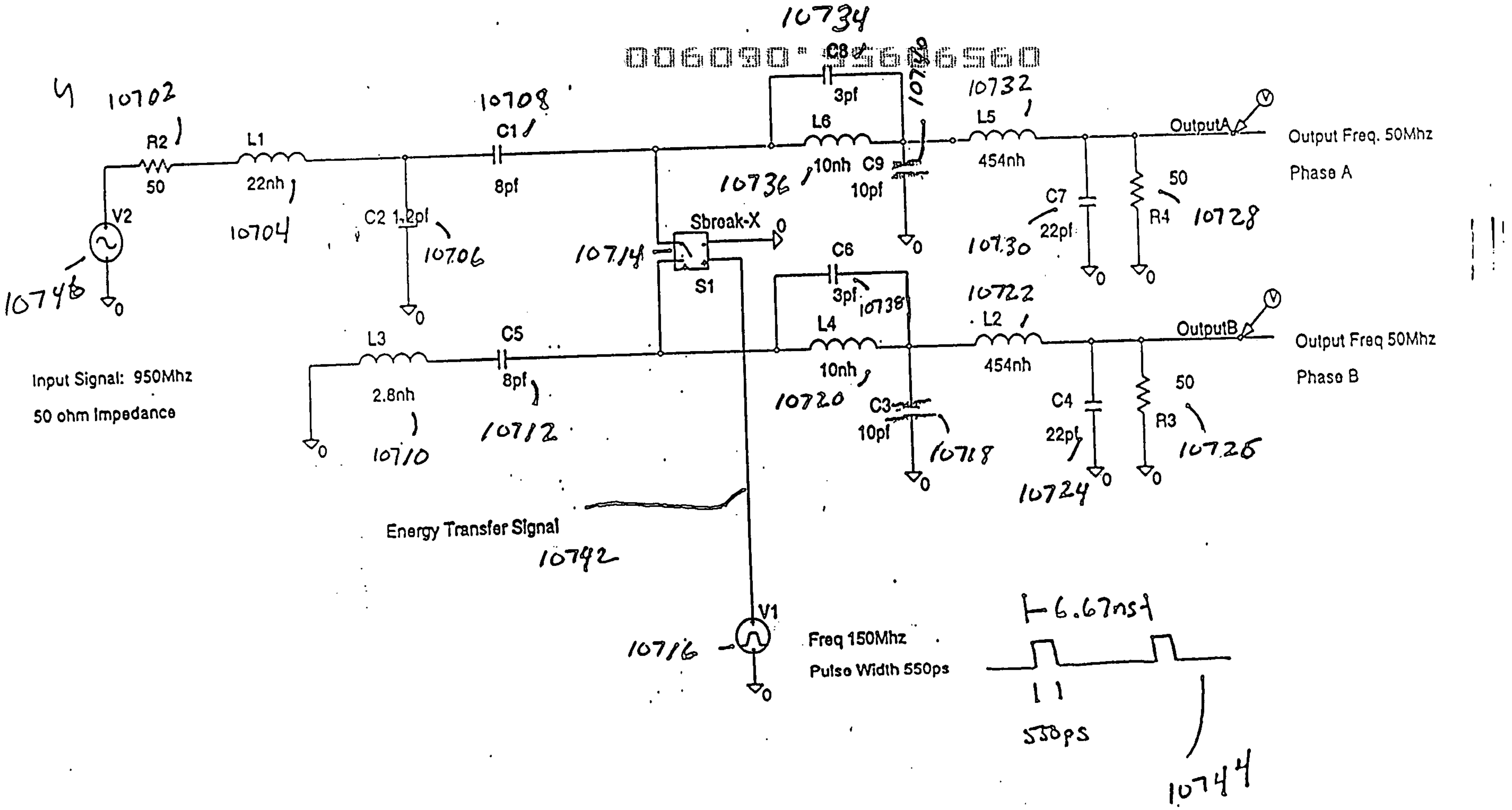


Fig. 106



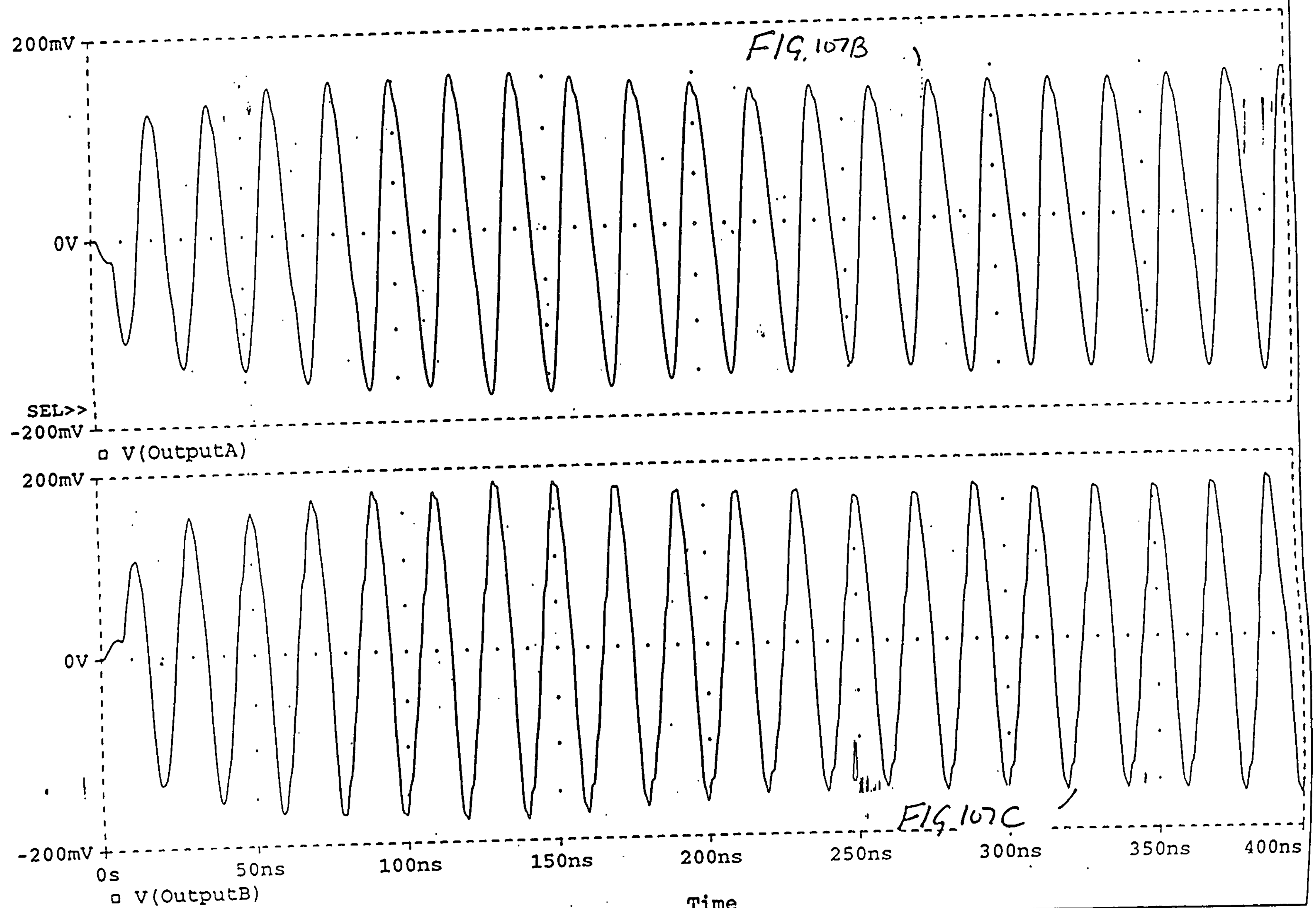
10702
10704
10706
10708
10710
10712
10714
10716
10718
10720
10722
10724
10726
10728
10730
10732
10734
10736
10738
10742
10744
10748
R2
50
L1
22nh
C2 1.2pf
C1
8pf
V2
Input Signal: 950Mhz
50 ohm Impedance
L3
2.8nh
C5
8pf
Sbreak-X
S1
C8
3pf
L6
10nh
C9
10pf
C6
3pf
L4
10nh
C3
10pf
L5
454nh
L2
454nh
C7
22pf
C4
22pf
R4
50
R3
50
OutputA
OutputB
Output Freq. 50Mhz
Phase A
Output Freq 50Mhz
Phase B
Energy Transfer Signal
V1
Freq 150Mhz
Pulse Width 550ps
6.67ns
550ps

FIG. 107A

Date/Time run: 10/14/98 15:37:54 * C:\MSim_8\Projects\Wireless\pat1.sch Temperature: 27.0

00609055606560

(A) pat1.dat



Date: October 14, 1998 Page 1 Time: 15:41:42

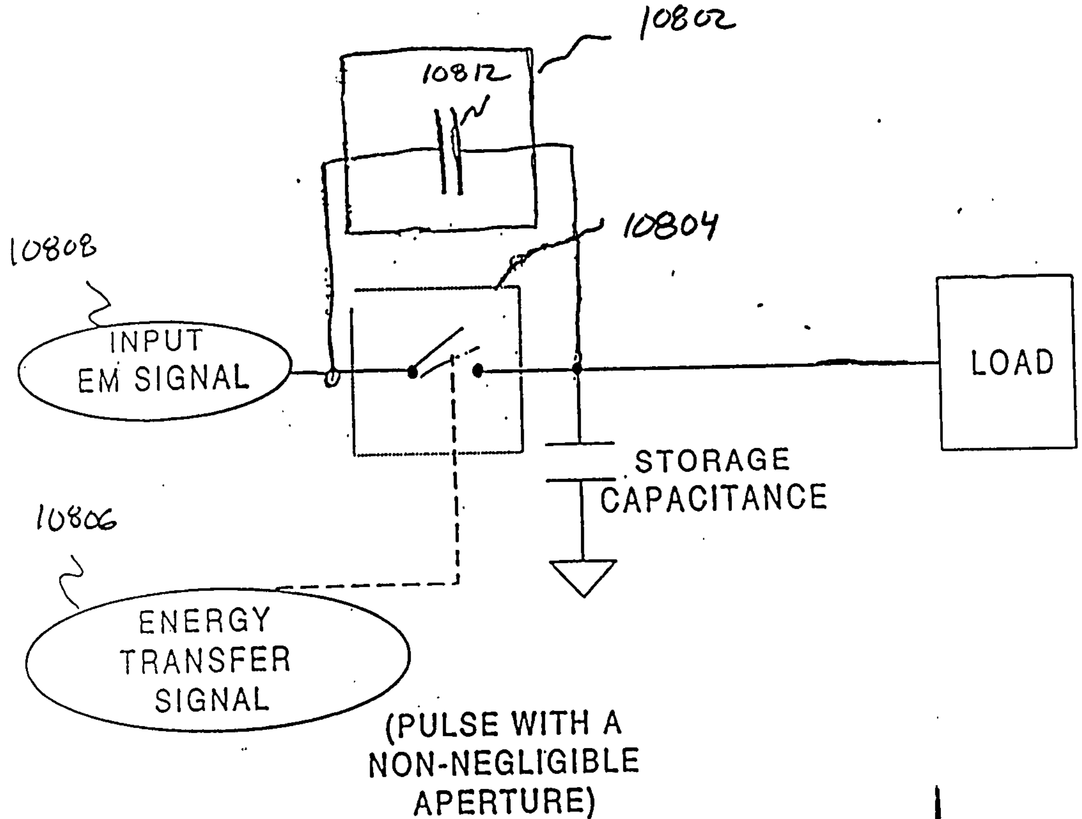

10802
10812
10804
10808
INPUT
EM SIGNAL
LOAD
STORAGE
CAPACITANCE
10806
ENERGY
TRANSFER
SIGNAL
(PULSE WITH A
NON-NEGLIGIBLE
APERTURE)

Fig. 108

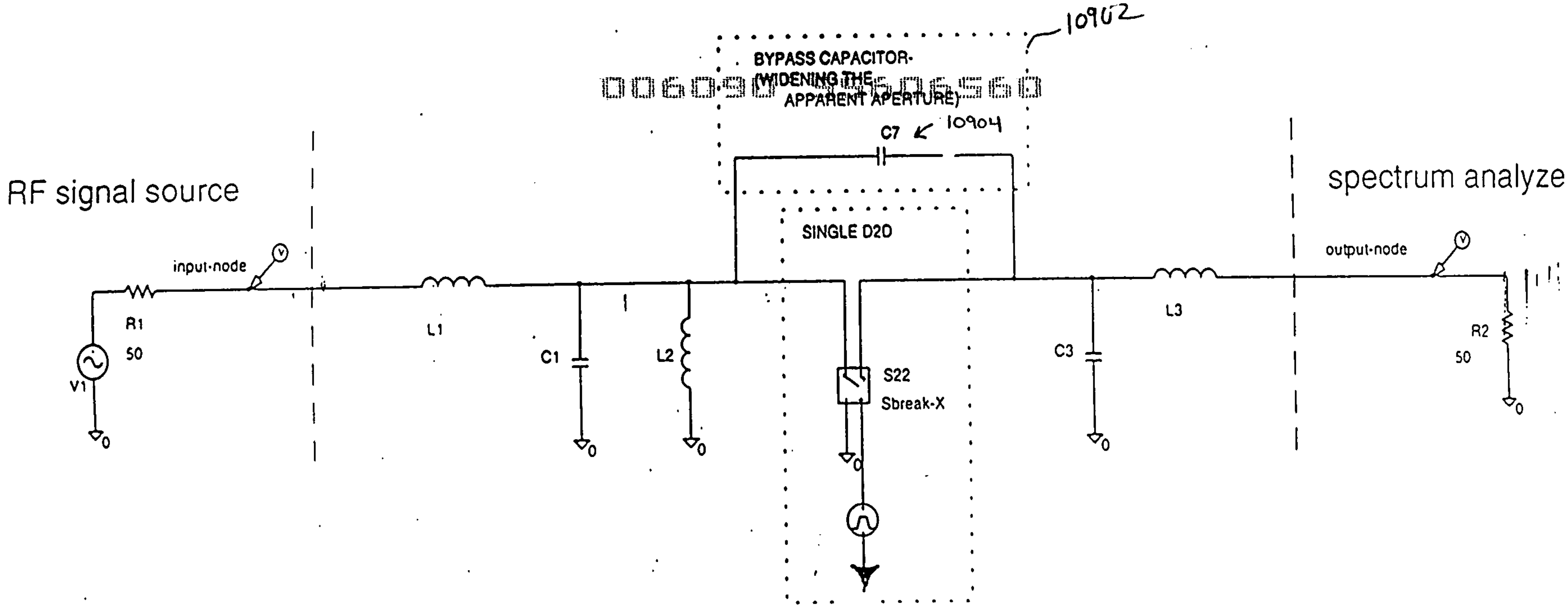

10902
BYPASS CAPACITOR-
(WIDENING THE
APPARENT APERTURE)
C7
10904
RF signal source
spectrum analyzer
SINGLE D2D
input-node
output-node
R1
50
V1
L1
C1
L2
S22
Sbreak-X
C3
L3
R2
50
0

FIG. 109

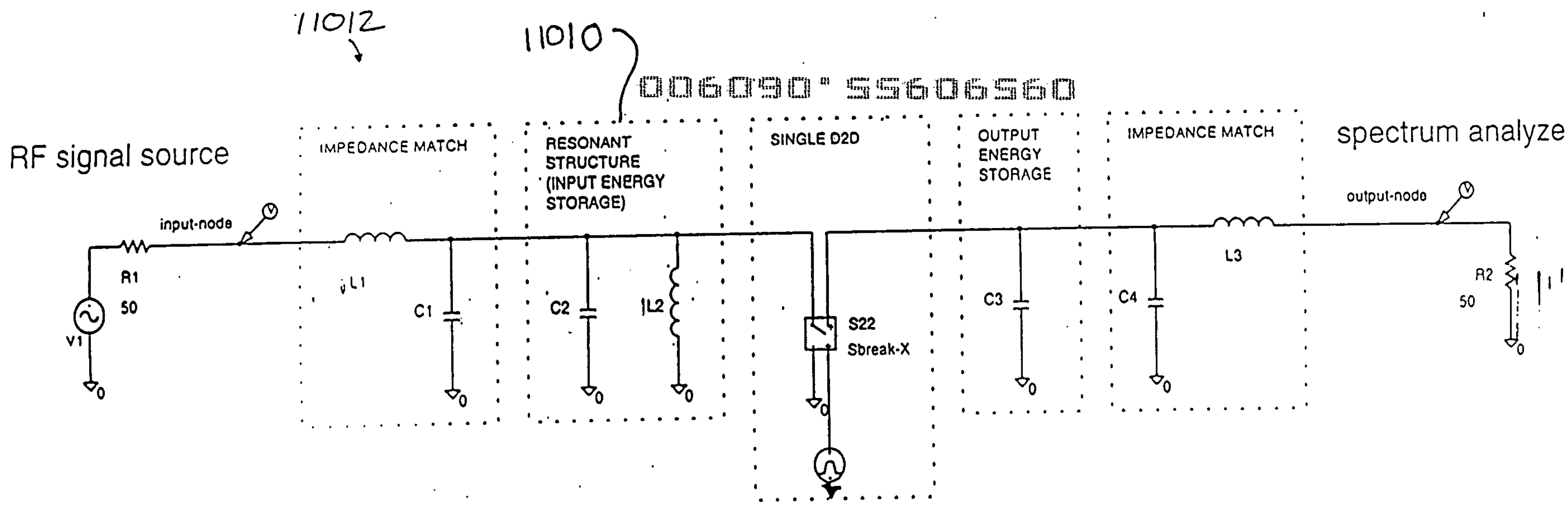
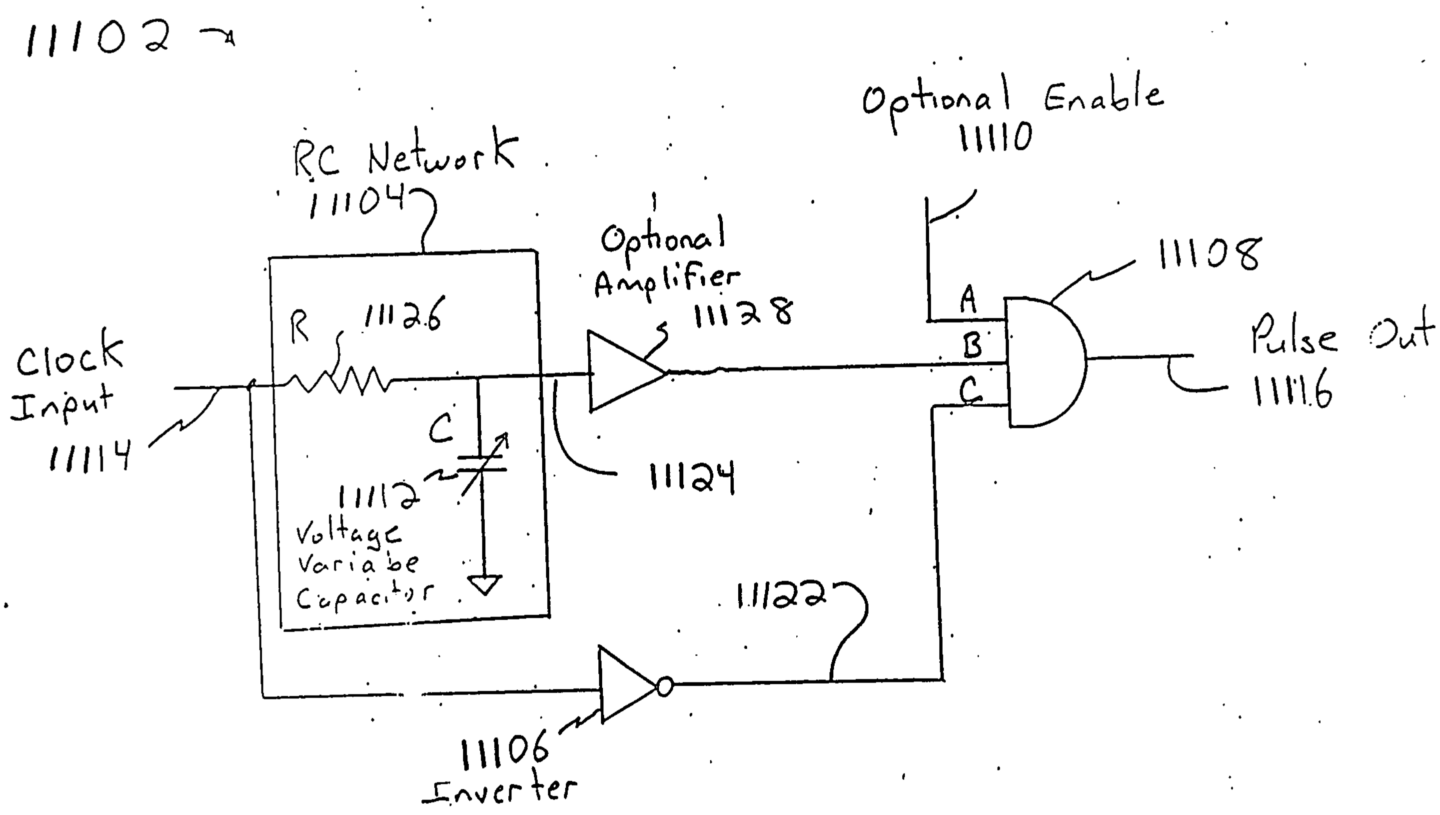

11012
11010
RF signal source
IMPEDANCE MATCH
RESONANT STRUCTURE (INPUT ENERGY STORAGE)
SINGLE D2D
OUTPUT ENERGY STORAGE
IMPEDANCE MATCH
spectrum analyzer
input-node
output-node
R1
50
V1
L1
C1
C2
L2
S22
Sbreak-X
C3
C4
L3
R2
50
0

FIG. 110



11102
RC Network
11104
Optional Enable
11110
Optional
Amplifier
11128
11108
R
11126
Clock
Input
11114
A
B
C
Pulse Out
11116
C
11112
Voltage
Variabe
Capacitor
11124
11122
11106
Inverter

FIG. 111A

006090" 55606560

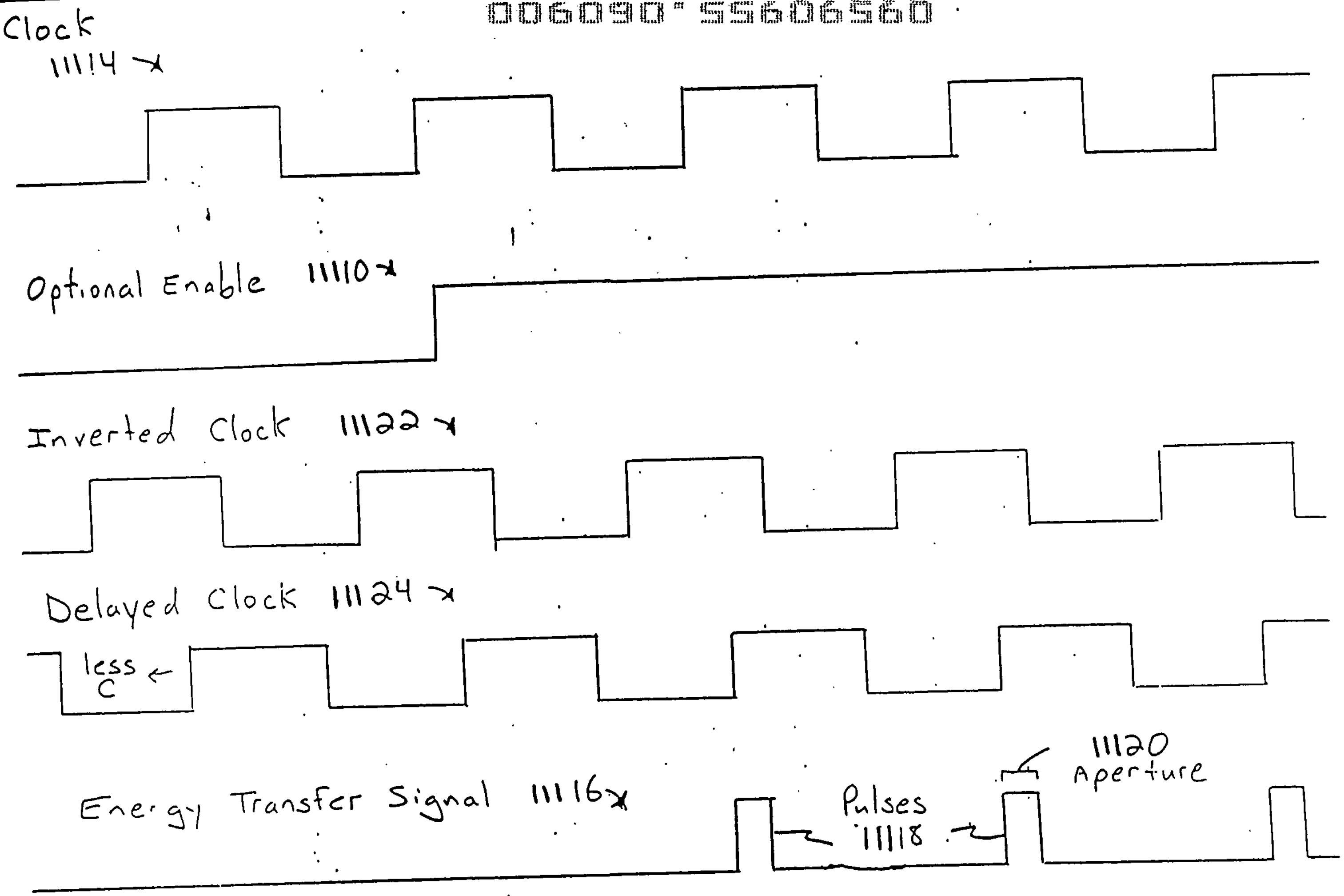


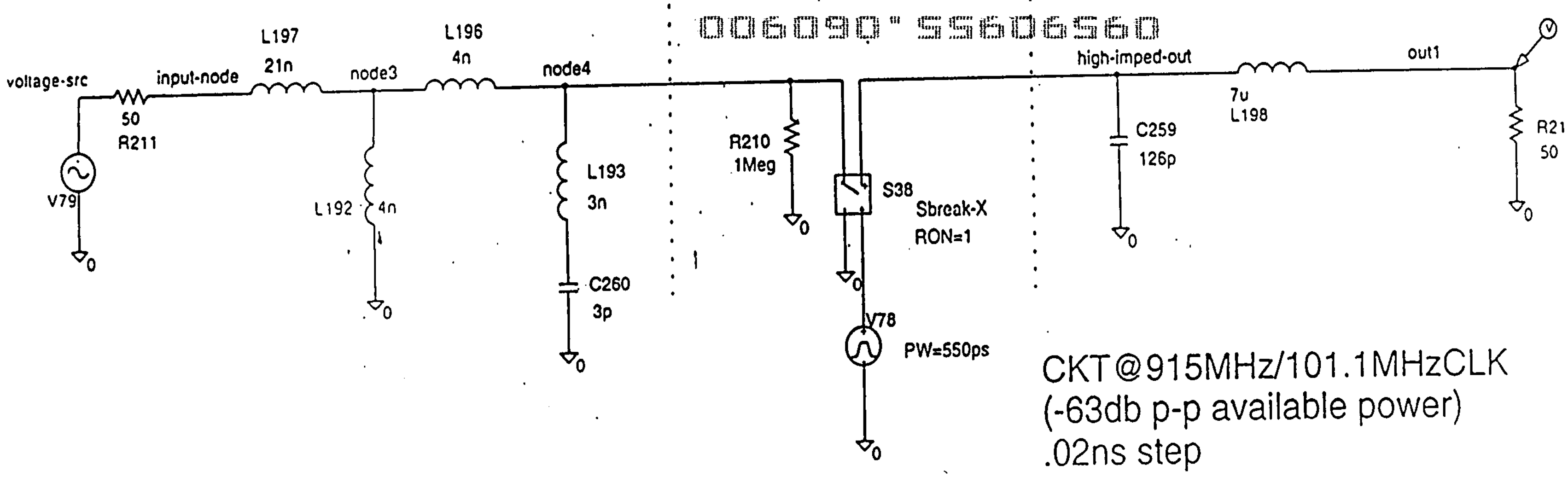
FIG 111B

FIG 111C

FIG 111D

FIG 111E

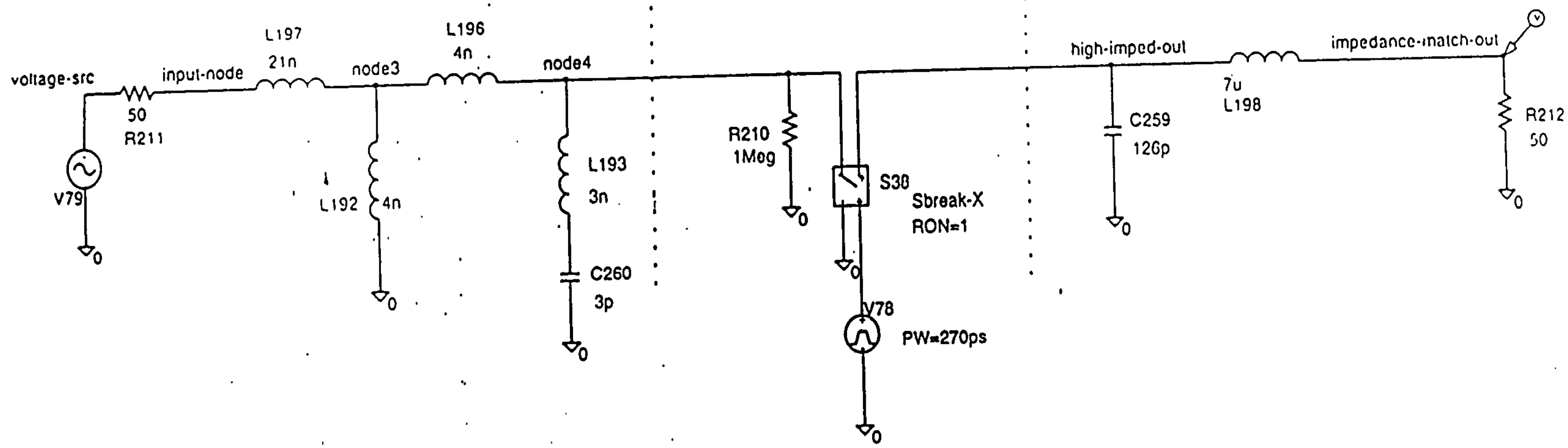
FIG 111F



CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-915M-5M-hieff.sch

FIG. 11/2

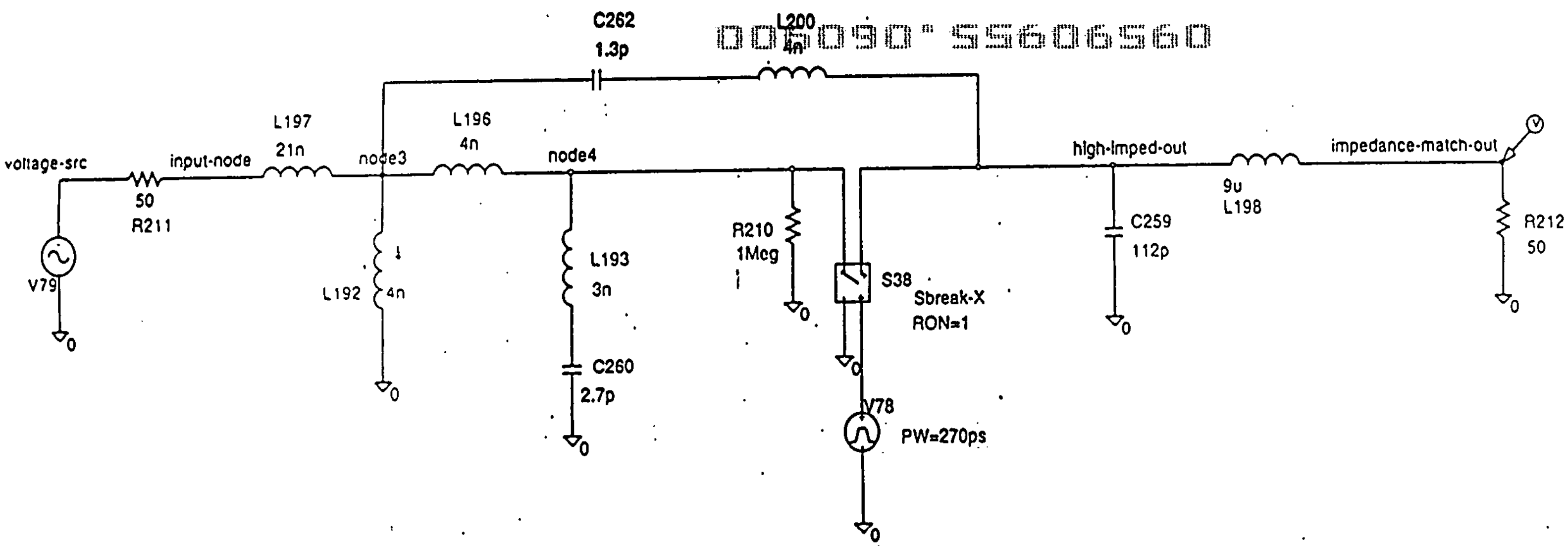


CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-smaperture915M-5M-hieff.sch

FIG. 113

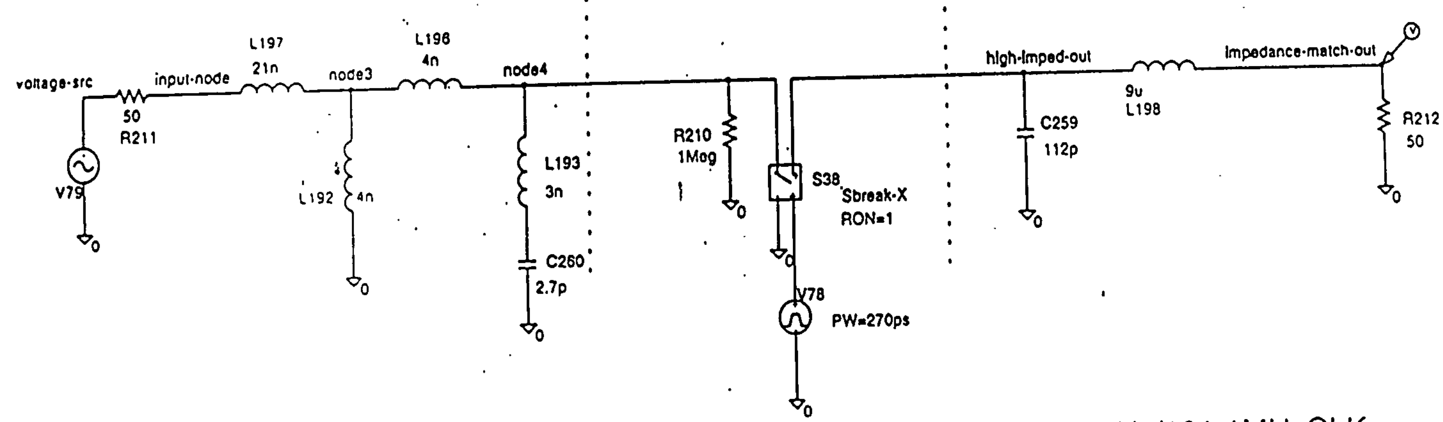
09955090 . 060600



CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-bypass-915M-5M-hieff.sch

FIG. 114



CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-wobypass-915M-5M-hieff.sch

FIG. 115

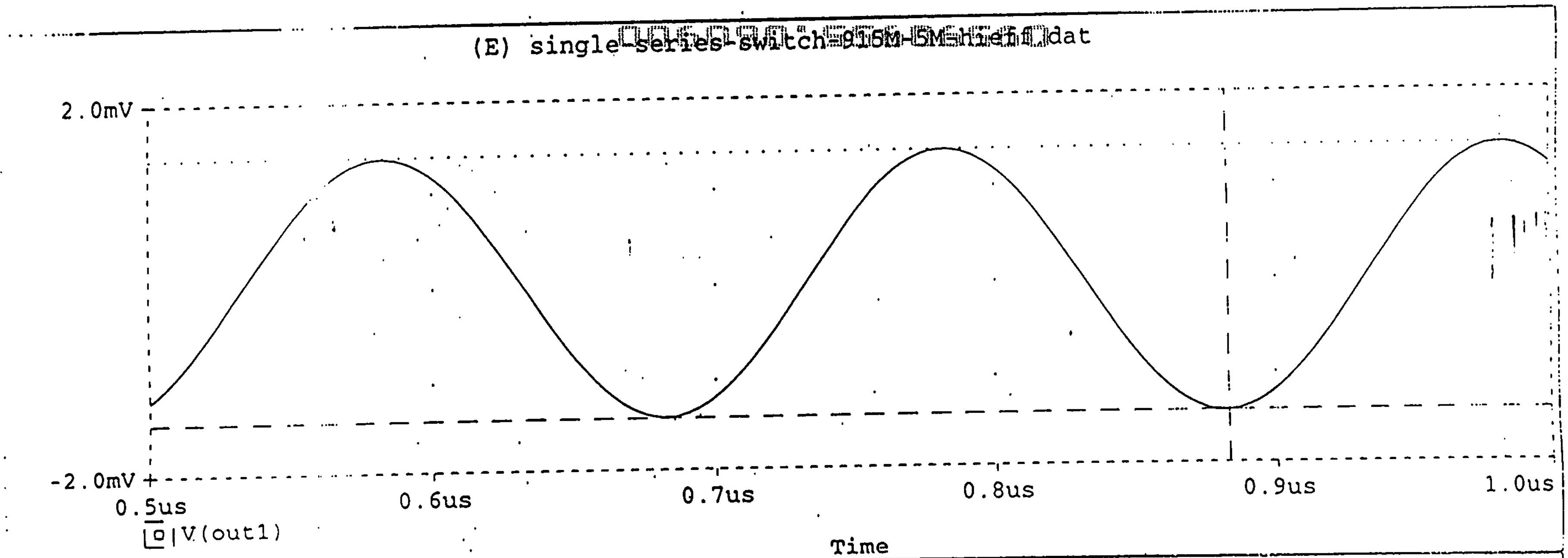


FIG. 116A

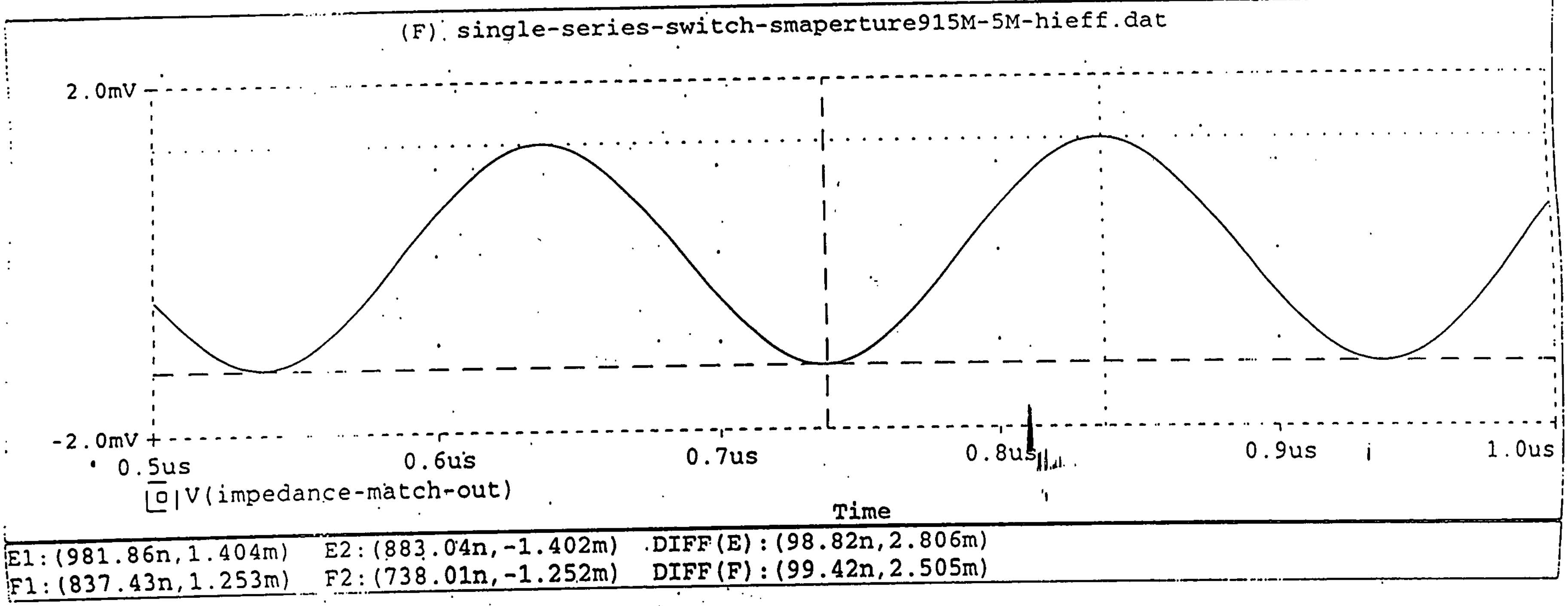


FIG. 116B

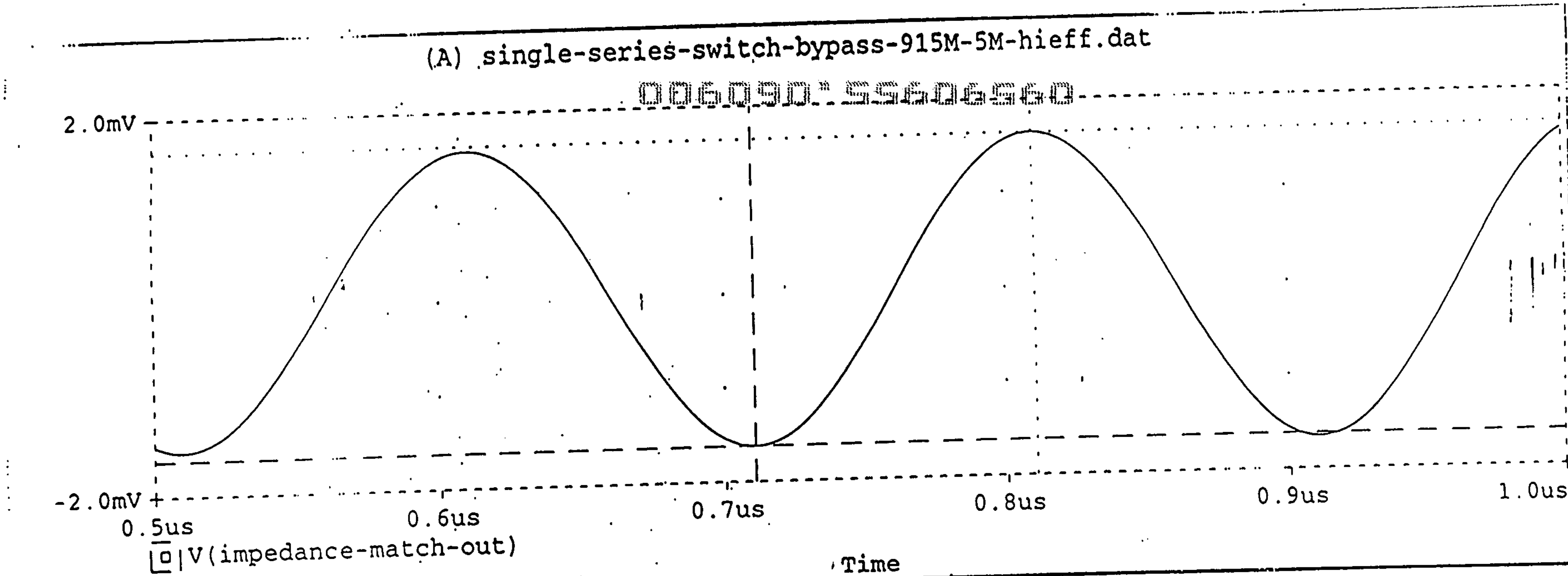


FIG. 117A

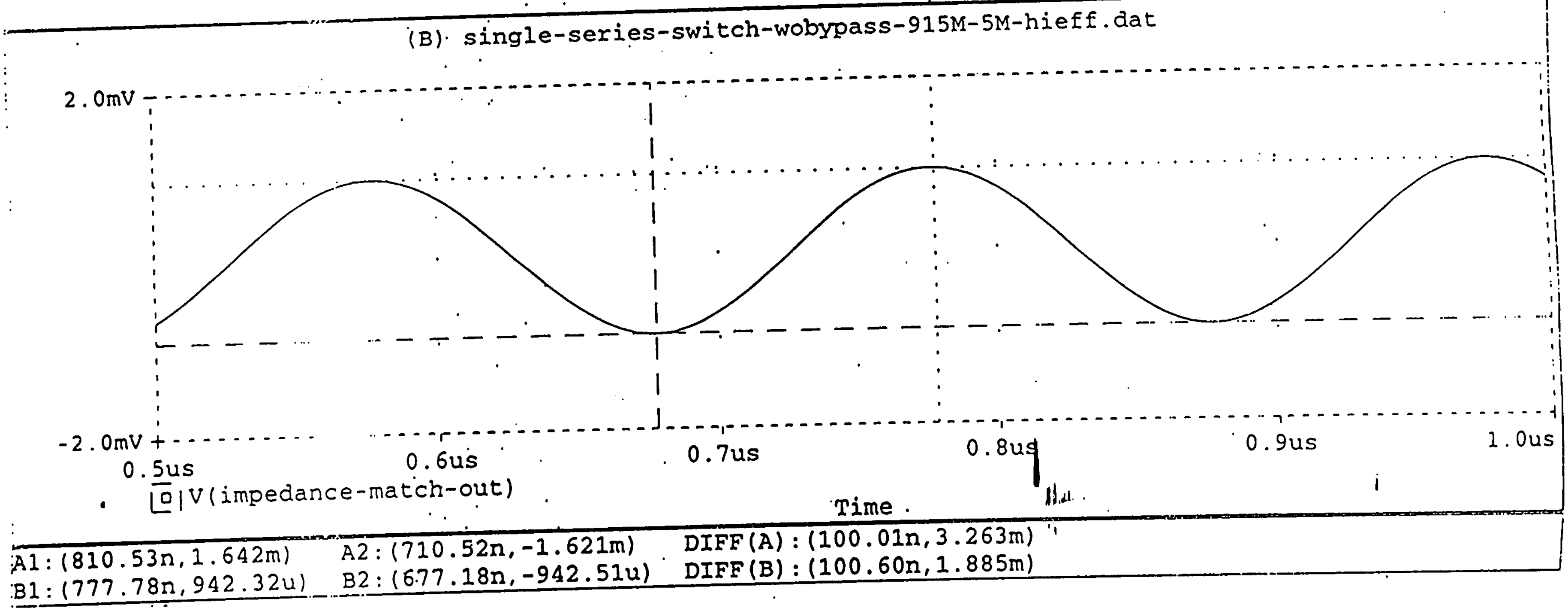


FIG. 117B

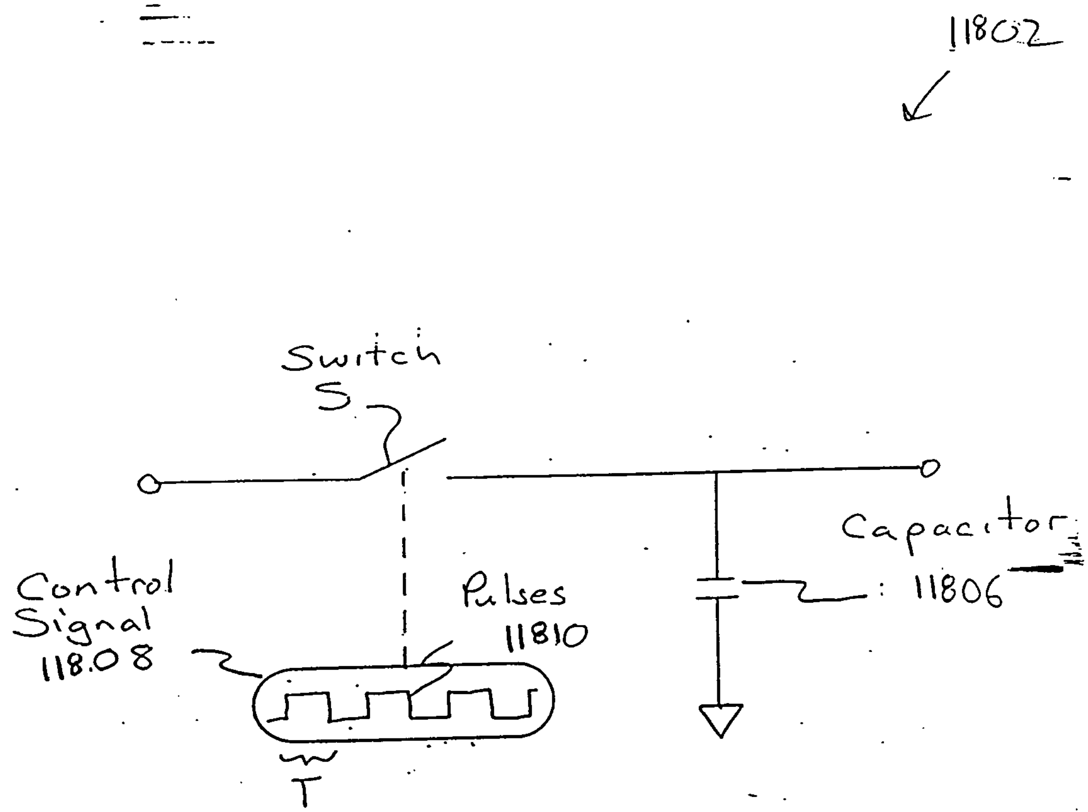

11802
Switch
S
Capacitor
11806
Control
Signal
118.08
Pulses
11810
T

FIG. 118A

$$q=C\cdot V \qquad \text{EQ. A}$$

$$V=A\cdot\sin(t) \qquad \text{EQ. B}$$

$$q(t)=C\cdot A\cdot\sin(t) \qquad \text{EQ. C}$$

$$\Delta q(t)=C\cdot A\cdot\sin(t)-C\cdot A\cdot\sin(t-T) \qquad \text{EQ. D}$$

$$\Delta q(t)=C\cdot A\cdot(\sin(t)-\sin(t-T)) \qquad \text{EQ. E}$$

$$\sin(\alpha)-\sin(\beta)=2\cdot\sin\left(\frac{\alpha-\beta}{2}\right)\cdot\cos\left(\frac{\alpha+\beta}{2}\right) \qquad \text{EQ. F.}$$

$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left[\frac{t-(t-T)}{2}\right]\cdot\cos\left[\frac{t+(t-T)}{2}\right] \qquad \text{EQ. G}$$

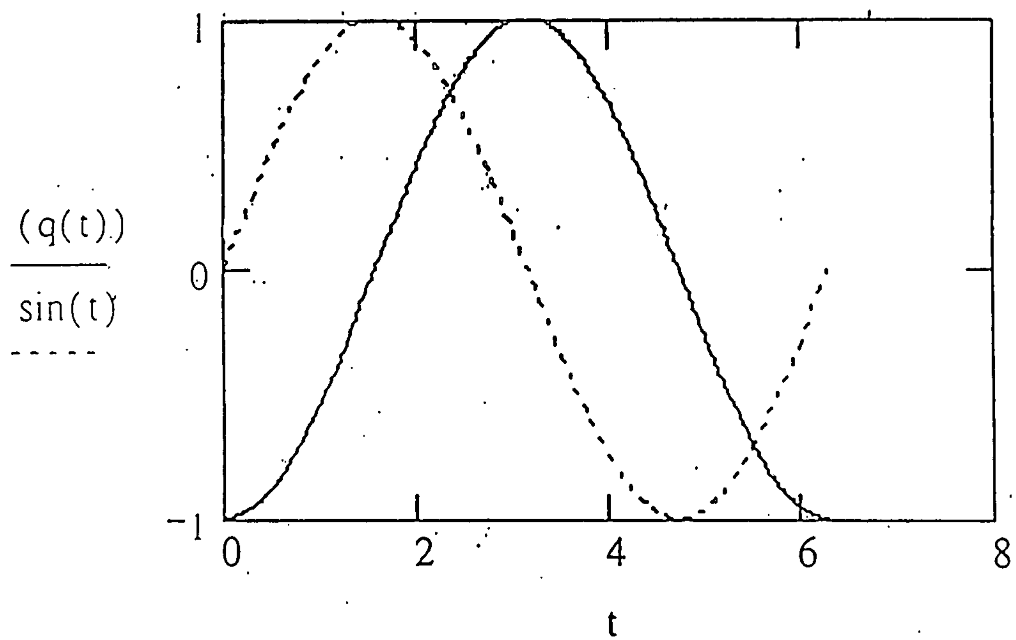
$$\Delta q(t)=2\cdot C\cdot A\cdot\sin\left(\frac{1}{2}\cdot T\right)\cdot\cos\left(t-\frac{1}{2}\cdot T\right) \qquad \text{EQ. H}$$

$$q(t)=\int C\cdot A\cdot(\sin(t)-\sin(t-T))\,dt \qquad \text{EQ. I}$$

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A \qquad \text{EQ. J}$$

$$q(t)=C\cdot A\cdot(\cos(t-T)-\cos(t)) \qquad \text{EQ. K}$$

FIG. 11B

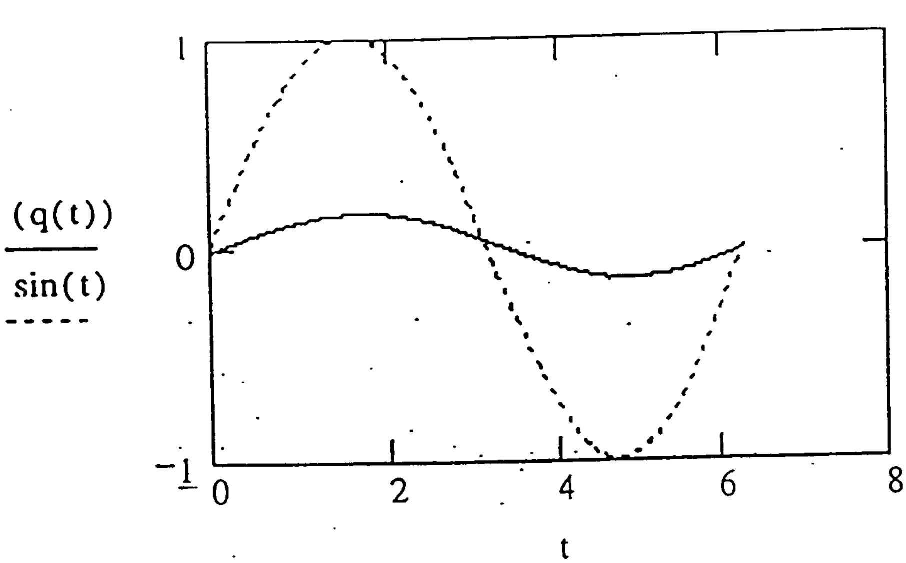


Graph 1

C=1;A=.5,T=¶

FIG. 118C

For Graph 2: C=1, A=.5, T=π/10:



Graph 2

FIG. 118D

Power - Charge Relationship

$$q = C \cdot V \qquad \text{EQ. L}$$

$$V = \frac{q}{C} \qquad \text{EQ. M}$$

$$V = \frac{J}{C} \qquad \text{EQ. N}$$

$$J = \frac{q^2}{C} \qquad \text{EQ. O}$$

$$P = \frac{J}{S} \qquad \text{EQ. P}$$

$$P = \frac{q^2}{C \cdot S} \qquad \text{EQ. Q}$$

FIG. 118E

Insertion Loss

Insertion loss in dB is expressed by:

$$ILdB = 10 \cdot \log\left(\frac{Pin}{Pout}\right)$$

or

$$ILdB = 10 \cdot \log\left[\frac{\left(\frac{Vin^2}{Rin}\right)}{\left(\frac{Vout^2}{Rout}\right)}\right]$$

FIG. 118F

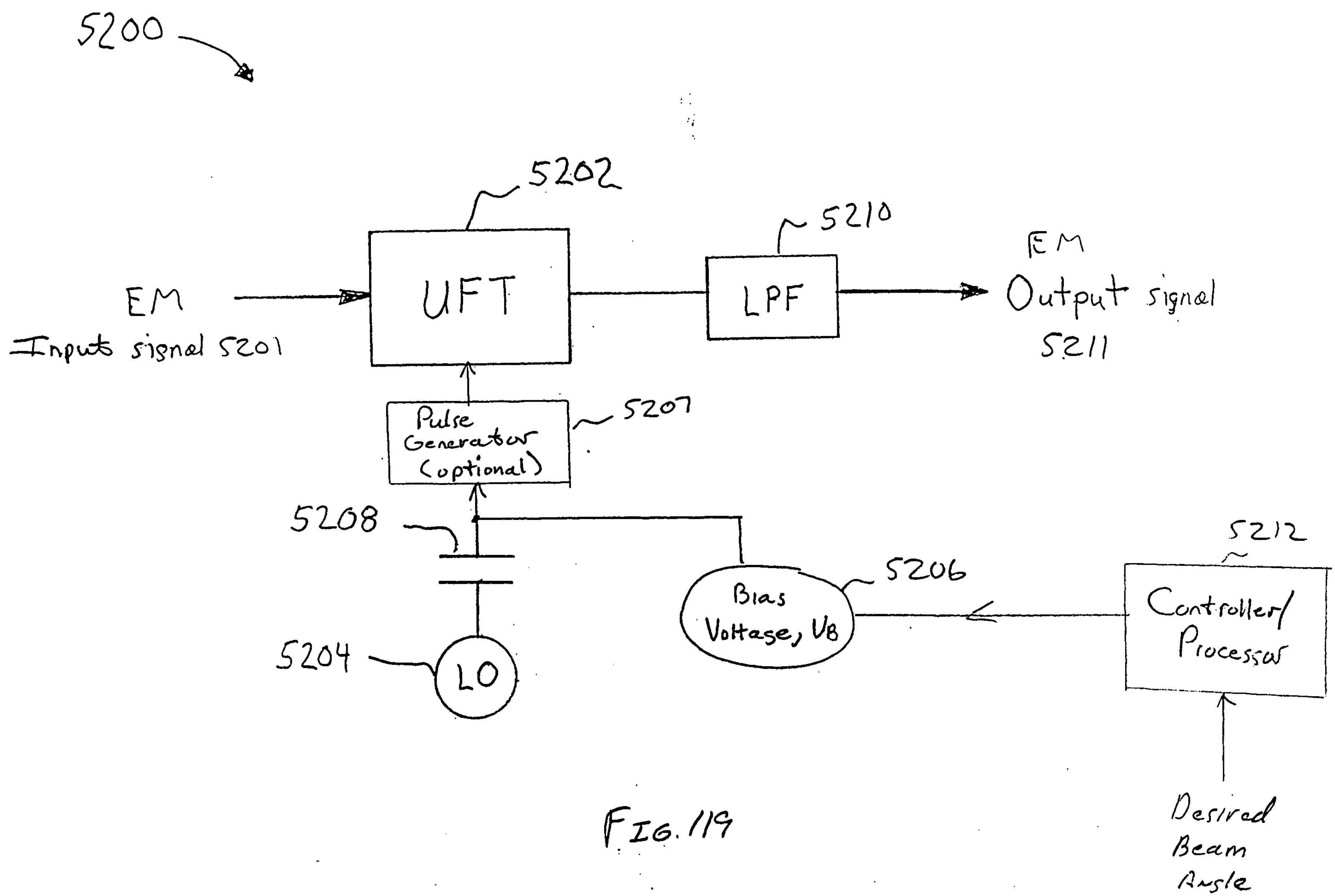

5200
5202
UFT
EM
Input signal 5201
5210
LPF
EM
Output signal
5211
Pulse Generator (optional)
5207
5208
5204
LO
Bias Voltage, V_B
5206
5212
Controller/ Processor
Desired Beam Angle

FIG. 119